Shanghai Fudan Microelectronics Group Company Limited

复旦微电子

FM24N256A

2-Wire Serial EEPROM

With Unique ID and Security Sector

Data Sheet

Jan. 2025

Trademarks

Description

The FM24N256A provides 262,144 bits of serial electrically erasable and programmable read-only memory (EEPROM) organized as 32,768 words of 8 bits each, with 128-bit UID and 64-byte Security Sector, and much improved the reliability by an internal ECC logic. The device's cascadable feature allows up to 8 devices to share a common 2-wire bus. The device is optimized for use in many industrial and commercial applications where low-power and low-voltage operations are essential.

Features

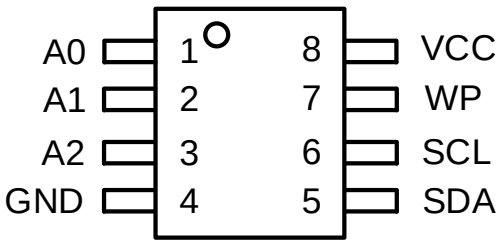
- **Low Operation Voltage: V_{CC} = 1.7V to 5.5V**
- **Internally Organized: 32,768 x 8**
- **2-wire Serial Interface**
- **Schmitt Trigger, Filtered Inputs for Noise Suppression**
- **Bi-directional Data Transfer Protocol**
- **High Speed Interface:**
  - **High-Speed Mode support for 3.4MHz**
  - **1MHz (Fast Mode Plus) and 400 kHz (Fast Mode) Compatibility**
- **Write Protect Pin for Hardware Data Protection**
- **64-Byte Page Write Modes (Partial Page Writes are Allowed)**
- **Lockable 64-Byte Security Sector**
- **128-Bit Unique ID for each device**
- **Self-timed Write Cycle (5ms max)**
- **Operating Temperature range:**
  - **-40°C to +85°C**
- **High-reliability**
  - **Endurance: 30 Million Write Cycles**
  - **Data Retention:100 Years**
  - **Built-in ECC Logic for Increased reliability**
  - **Enhance ESD Protection:⩾4KV**
  - **Prevention of Write Mistake at Low Voltage**
- **SOP8, TSSOP8 and TDFN8 Packages (RoHS Compliant and Halogen-free)**

Pin Configurations

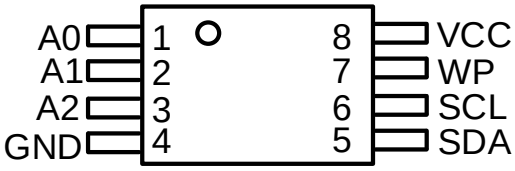
Pin Name	Function
A0~A2	Device Address Inputs
SDA	Serial Data Input/Output
SCL	Serial Clock Input
WP	Write Protect
V_{CC}	Power Supply
GND	Ground

Packaging Type

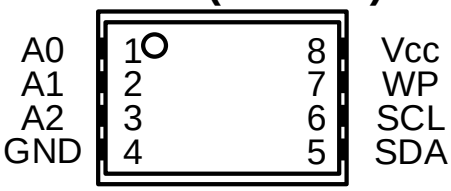
SOP 8



TSSOP8



TDFN8(2×3mm)

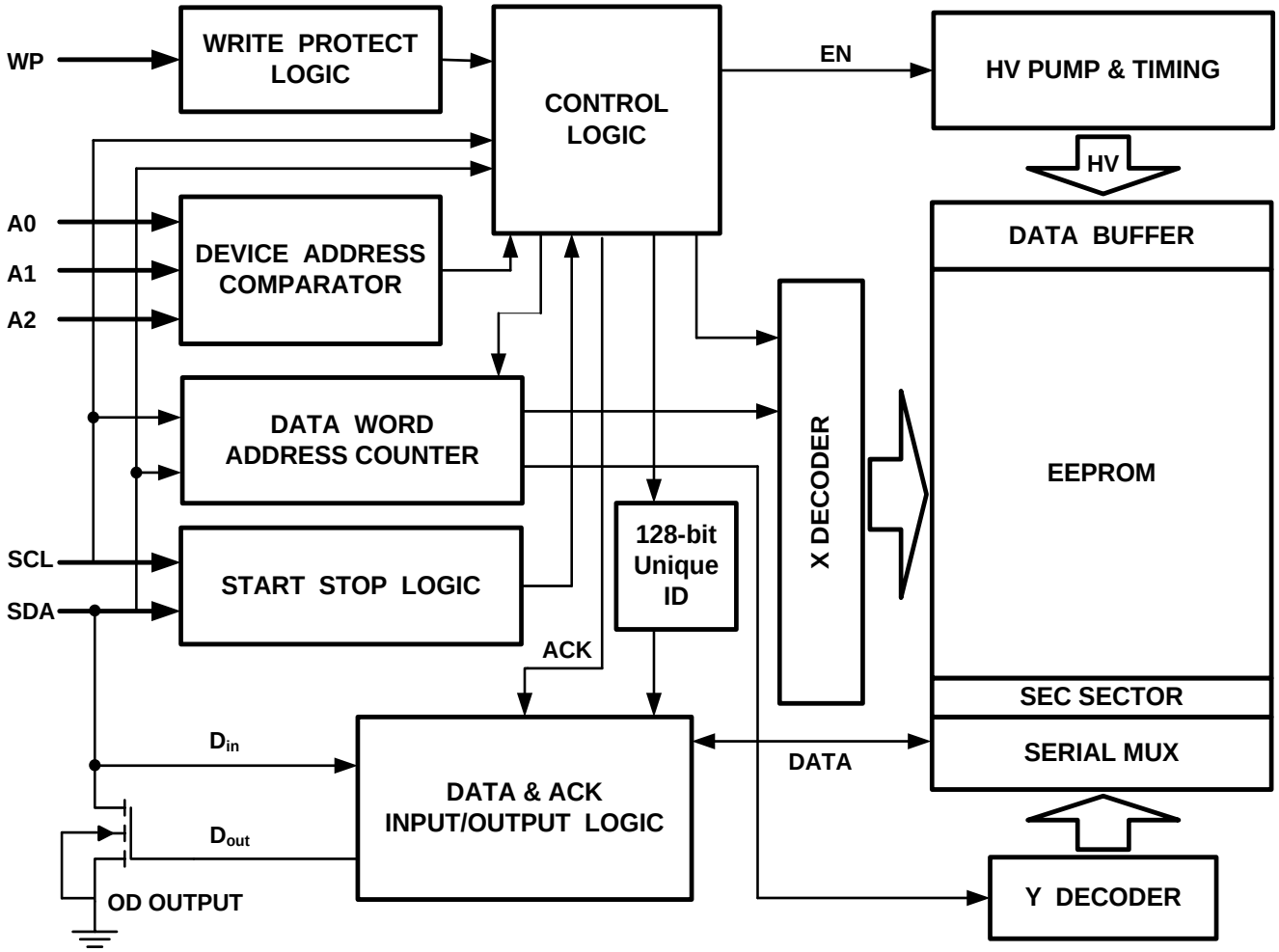


Absolute Maximum Ratings

Ambient Operating Temperature	-55℃ to +125℃
Storage Temperature	-65℃ to +150℃
Voltage on Any Pin with Respect to Ground	-0.5V to +7.0V
Maximum Operating Voltage	6.25V
DC Output Current	5.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

Figure 1. Block Diagram



Pin Description

SERIAL CLOCK (SCL): The SCL input is used to positive edge clock data into each EEPROM device and negative edge clock data out of each device.

SERIAL DATA (SDA): The SDA pin is bi-directional for serial data transfer. This pin is open-drain driven and may be wire-ORed with any number of other open-drain or open-collector devices.

DEVICE/PAGE ADDRESSES (A2, A1, A0): The A2, A1 and A0 pins are device address inputs that are hardwired or left not connected for hardware compatibility with other FM24CXX / FM24NXX devices. When the pins are hardwired, as many as eight 256K devices may be addressed on a single bus system (device addressing is discussed in detail under the Device Addressing section). If the pins are left floating, the A2, A1 and A0 pins will be internally pulled down to GND if the capacitive coupling to the circuit board V_{CC} plane is <3pF, if coupling is >3pF, FMSH recommends connecting the address pins to GND.

WRITE PROTECT (WP): The FM24N256A has a Write Protect pin that provides hardware data protection. The WP pin allows normal write operations when connected to ground (GND). When the Write Protect pin is connected to VCC, all write operations to the memory are inhibited. If the pin is left floating, the WP pin will be internally pulled down to GND if the capacitive coupling to the circuit board Vcc plane is <3pF. If coupling is >3pF, FMSH recommends connecting the WP to GND. Switching WP to V_{CC} prior to a write operation creates a software write protected function.

Power-up Timing Requirements

To prevent write operations or other spurious events from occurring during power-up, the FM24N256A includes a power-on reset (POR) circuit.

The system designer must ensure that instructions are not sent to the device until the Vcc supply has reached a stable value, greater than or equal to the minimum Vcc level. Additionally, once the Vcc is greater than or equal to the minimum Vcc level, the host must wait at least t_{INIT} before sending the first command to the device. See Table 1 for the values associated with these power-up parameters.

If an event occurs in the system where the Vcc level supplied to the FM24N256A drops below the maximum V_{POR} level specified, it is recommended that a full-power cycle sequence be performed by first driving the Vcc pin to Vss, waiting at least the minimum t_{POFF} time and then perform a new power-up sequence in compliance with the requirements defined in Table 1.

During a power-up sequence, the Vcc supplied to the FM24N256A should monotonically rise from Vss to the minimum Vcc level, as specified in Table 1.

Figure 2. V_{CC} Ramp Up and Ramp Down

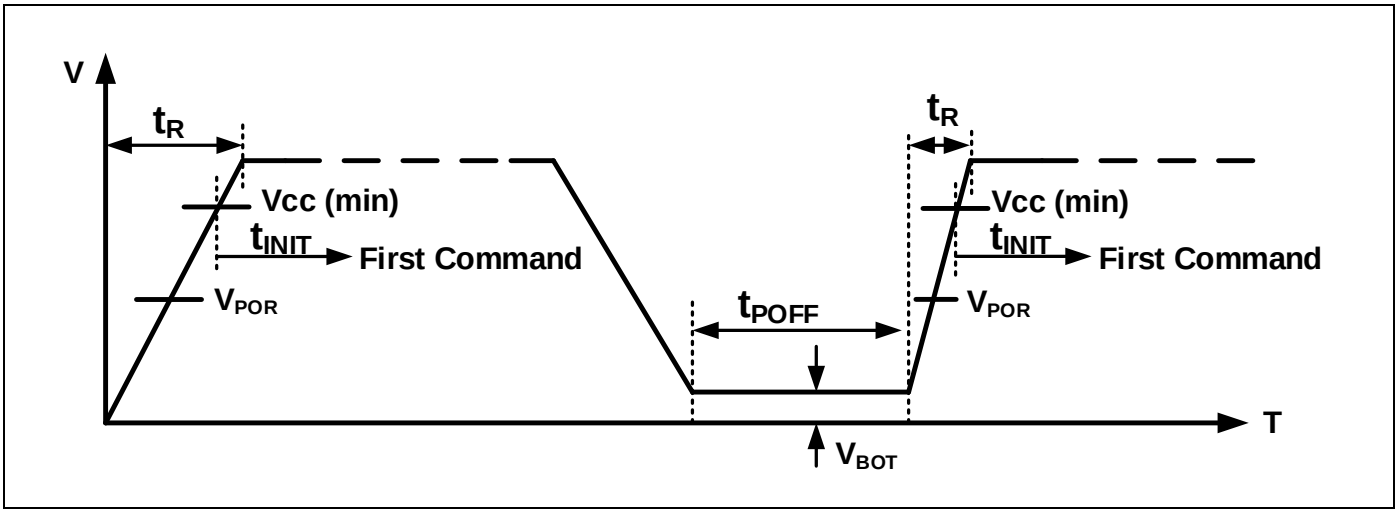


Table 1. Power-up conditions

Symbol	Parameter	Test Condition	Min	Max	Units
t_R	Power on time		0.001	2000	ms
t_{POFF}	power cycle off time		300		µs
t_{INIT}	Time from power on to first command		1		ms
V_{BOT}	Power Off threshold for the next power on cycle	No ringback above V_{Bot}		0.7	V
V_{POR}	Power-On Reset threshold voltage			1.3	V

Note: VCC must rise monotonically without ringback.

Low Voltage Malfunction Prevention Function

The FM24N256A has a built-in detection circuit which prevents data rewrite operation at low power, and prevents write or read operation error. At VDET or lower, rewriting of data is prevented (Refer to Figure 3).

Figure 3. Operation during Low Power Supply Voltage

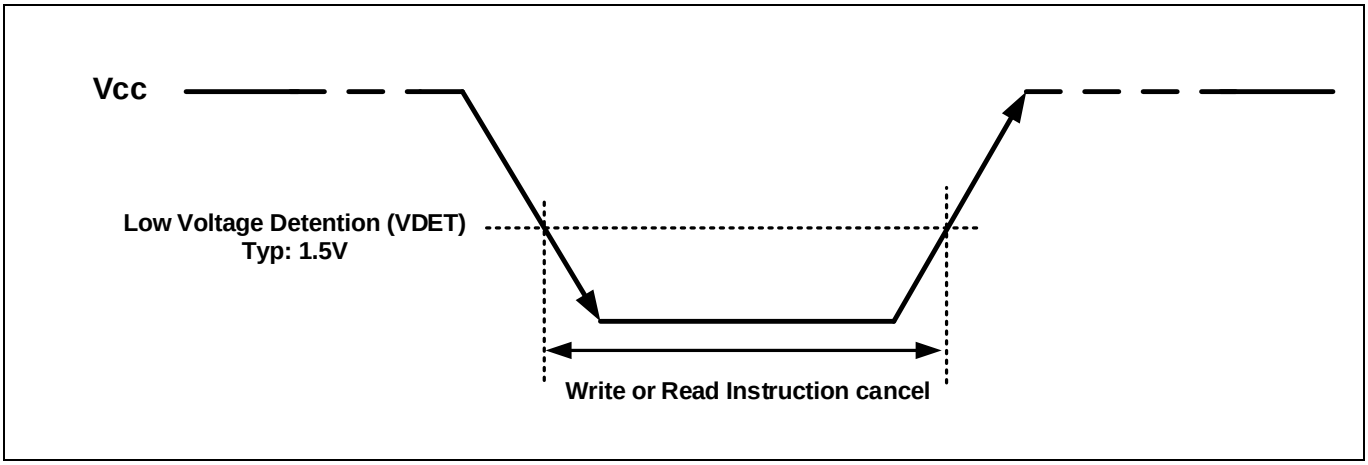


Table 2. V_{DET} parameters

Symbol	Parameter	Test Condition	Min	Max	Units
V_{DET}	Low power detention voltage			1.55	V

Write Protect Description

Table 3. Write Protection

WP Pin Status	Part of the Memory Protected
WP=V_{CC}	Full Memory
WP=GND	Normal Read/Write Operations

When the WP pin is connected to the V_{CC}, write operation to memory area is inhibited. When the WP pin is connected to GND or set in open, the write protect is invalid, and write operation in all memory area is available.

Write-protect condition: The WP pin must be connected to V_{CC} from start condition in the write operation (byte write, page write) until stop condition (refer to Figure 13).
If the WP pin changes during this time, the address data being written at this time is not guaranteed. Regarding the timing of write protect, refer to Figure 6.

Non-write-protect condition: The WP pin must be connected to GND from start condition in the write operation (byte write, page write) until stop condition (refer to Figure 14).

When not using write protection, connect the WP pin to GND or leave it floating. The write protection is valid within the operating power supply voltage range. As seen in Figure 13 when the write protection is valid, the EEPROM does not acknowledge (NoACK) after data input and does not start a write operation after the stop condition.

High-Speed Mode

The FM24N256A supports the High-Speed (HS) mode allowing it to operate at clock frequencies up to 3.4MHz for read and write operations.

To activate HS mode for the FM24N256A, the host should first initiate a Start condition. Then, following Table 4, the reserved HS mode host code of '00001xxxb' must be used.

Table 4. High-Speed Mode Host Code

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Ack Bit
0	0	0	0	1	x	x	x	NoACK from Clients
MSB							LSB	

NOTE: x = Don`t care bit.

The host code in HS mode should be sent to the device at Fast mode plus (1 MHz) or slower clock frequencies. The FM24N256A will not acknowledge (NoACK) the HS mode host code because it is meant to be recognized by all client devices that support the HS mode.

Once the FM24N256A receives the HS mode host code and the NoACK occurs, the FM24N256A will relax its input filters on SDA and SCL to the HS mode tolerance to accept transfers, at up to 3.4MHz. The device will then enter HS mode and wait for a Repeated Start condition before the next operation can occur.

Next, the host must issue a Start condition, followed by a valid device address byte to which the device will ACK. The host can continue with read or write operations at the higher clock speed and the FM24N256A will continue to operate in the HS mode until one of the following events occurs:

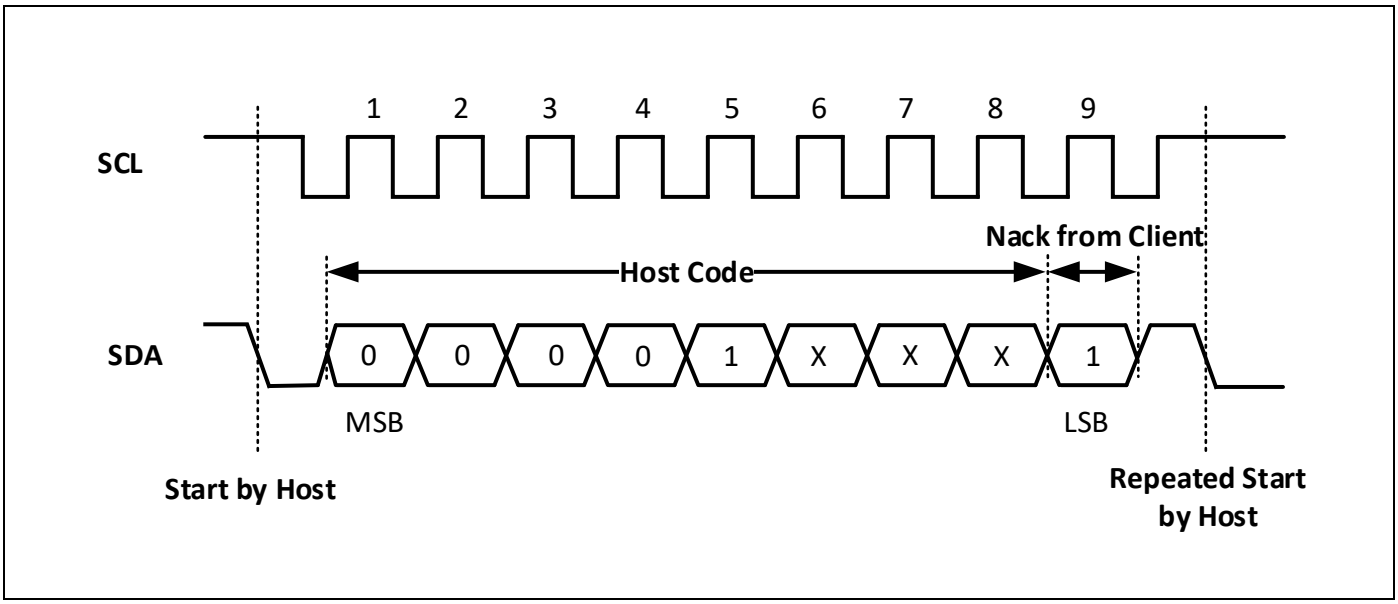
1. The host sends a Stop condition. Therefore, the host should use a Repeated Start condition to begin new HS mode operations rather than a Stop - Start sequence.

2. A Power-On-Reset (POR) event occurs.

Note :

1. The internal write cycle requires a Stop condition to be sent after the last data byte. This Stop condition will cause the FM24N256A to exit HS mode. Therefore, if more than one page of data is to be written, HS mode must be re-entered for every write operation.
2. Once the FM24N256A exits the HS mode from one of these events, the device will switch its input and output filters back to the standard I^2C (Legacy) mode. Figure 4 illustrates the HS mode entry sequence.
3. High-Speed mode entry is ignored during a write cycle. Therefore, polling must occur while using Fast mode plus (1MHz) or slower clock frequencies. Refer to Acknowledge Polling for additional information on page 19. HS mode can be re-entered after the write cycle has completed.

Figure 4. High-Speed Mode Entry Sequence



Memory Organization

FM24N256A, 256K SERIAL EEPROM: Internally organized with 512 pages of 64bytes each, the 256K requires a 16-bit data word address for random word addressing.

Security Sector: The FM24N256A offers 64-byte Security Sectors which can be written and (later) permanently locked in Read-only mode. This memory may be used by the system manufacturers to store security and other important information separately from the main memory array.

Unique ID: The FM24N256A utilizes a separate memory block containing a factory programmed read-only 128-bit unique ID.

Table 5. Memory Organization

Device ADDR	Page ADDR	Byte Number		
		63	…	0
1010	0	Data Memory (512P X 64B)		
	1			
	2			
	…			
	511			
1011	xxxx x00x xxxx xxxx[1]	Security Sector (64Bytes)		
1011	xxxx x01x xxxx xxxx[2]	Unique ID（128 Bits）		

Note: 1. Address bits ADDR<10:9> must be 00, ADDR<5:0> define byte address, other bits are don't care
2. Address bits ADDR<10:9> must be 01, ADDR<3:0> define byte address, other bits are don't care

Pin Capacitance

Table 6. Pin Capacitance parameters

SYMBOL	PARAMETER	CONDITIONS	Max	Units
C_{IN} [1]	Input Capacitance	V_{IN} = 0V, f = 1MHz	6	pF
C_{OUT} [1]	Output Capacitance	V_{OUT} = 0V, f = 1MHz	8	pF

Note: 1. This parameter is characterized and is not 100% tested.

Cycling Performance

Table 7. Cycling performance

SYMBOL	PARAMETER	TEST CONDITIONS	Min	Units
Write cycle endurance (Group Mode) Note2	Ncycle	$V_{CC(min)} < V_{CC} < V_{CC(max)}$	4,000,000	Write cycle
Write cycle endurance (Page Mode) Note3		$V_{CC(min)} < V_{CC} < V_{CC(max)}$	30,000,000	Write cycle

Note:

1. This parameter is characterized and qualification. It is not 100% tested.
2. Group Mode:
   - The Write cycle endurance is defined for groups of four data bytes located at addresses [4*N, 4*N+1, 4*N+2, 4*N+3] where N is an integer.
   - A Write cycle is executed when either a Page Write, a Byte Write, a Write Security Sector or a Lock Security instruction is decoded. When using these instructions, refer also to Section: Cycling with Error Correction Code (ECC) on page 19.
3. Page Mode: The write cycle endurance is defined for a full page of 64bytes.

Data Retention

Table 8. Data Retention

PARAMETER	Test Condition	Min	Units
Data retention	T_A = 55 °C	100	Year

Note:
1. This parameter is characterized and qualification. It is not 100% tested.

DC Characteristics

Table 9. DC Characteristics

Applicable over recommended operating range from: T_A = -40℃ to +85℃, V_{CC} = +1.7V to +5.5V, (unless otherwise noted).

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
V_{CC}	Supply Voltage		1.7		5.5	V
I_{CC1}	Supply Current	V_{CC} = 5.0V, Read at 400KHz		0.2	0.5	mA
I_{CC2}	Supply Current	V_{CC} = 5.0V, Write at 400KHz		1.0	3.0	mA
I_{SB1}	Standby Current	V_{CC} = 1.7V, V_{IN} = V_{CC}/ V_{SS}		0.1	1.0	µA
I_{SB2}	Standby Current	V_{CC} = 5.5V, V_{IN} = V_{CC}/ V_{SS}		0.6	6.0	µA
I_{LI}	Input Leakage Current	V_{IN} = V_{CC}/V_{SS}		0.05	2.0	µA
I_{LO}	Output Leakage Current	V_{OUT} = V_{CC}/ V_{SS}		0.05	2.0	µA
V_{IL}[1]	Input Low Level		-0.45		V_{CC} x 0.3	V
V_{IH}[1]	Input High Level		V_{CC} x 0.7		V_{CC} + 0.5	V
V_{OL2}	Output Low Level 2	V_{CC} = 3.0V, I_{OL} = 2.1 mA			0.4	V
V_{OL1}	Output Low Level 1	V_{CC} =1.7V, I_{OL} = 0.15 mA			0.2	V

Note: 1. V_{IL} min and V_{IH} max are reference only and are not tested.

AC Characteristics

Table 10. Fast-Mode(400kHz) and Fast-Mode Plus(1MHz) AC characteristics

Recommended operating conditions: T_A = -40℃ to +85℃, V_{CC} = +1.7V to +5.5V, CL = 100 pF (unless otherwise noted). Test conditions are listed in Note 2.

Symbol	Parameter	400KHz Fast Mode		1MHz Fast Mode Plus		Units
		Min	Max	Min	Max	
f_{SCL}	Clock Frequency, SCL		400		1000	kHz
t_{LOW}	Clock Pulse Width Low	1.3		0.5		µs
t_{HIGH}	Clock Pulse Width High	600		260		ns
t_I [1]	Noise Suppression Time		50		50	ns
t_{AA}	Clock Low to Data Out Valid	100	900	100	450	ns
t_{BUF} [1]	Time the bus must be free before a new transmission can Start	1.3		0.5		µs
$t_{HD.STA}$	Start Hold Time	600		250		ns
$t_{SU.STA}$	Start Setup Time	600		250		ns
$t_{HD.DAT}$	Data In Hold Time	0		0		µs
$t_{SU.DAT}$	Data In Setup Time	100		50		ns
t_R	Inputs Rise Time [1]		300		120	ns
t_F	Inputs Fall Time [1]		300		120	ns
$t_{SU.STO}$	Stop Setup Time	600		250		ns
t_{DH}	Data Out Hold Time	100		100		ns
t_{WS1}	WP setup time	1		1		µs
t_{WH1}	WP hold time	1		1		µs
t_{WS2}	WP release setup time	1		1		µs
t_{WH2}	WP release hold time	1		1		µs
t_{WR}	Write Cycle Time		5		5	ms

Notes: 1. This parameter is characterized and is not 100% tested.

2. AC measurement conditions:

RL (connects to V_{CC}): 1.3 kΩ

Input pulse voltages: 0.3 V_{CC} to 0.7 V_{CC}

Input rise and fall times: ≤ 50 ns

Input and output timing reference voltages: 0.5 V_{CC}

Table 11. High-Speed Mode(3.4MHz) AC characteristics

Recommended operating conditions: T_A = -40℃ to +85℃, V_{CC} = +2.5V to +5.5V, CL = 100 pF (unless otherwise noted). Test conditions are listed in Note 3.

Symbol	Parameter	Min	Max	Units
f_{SCL}	Clock Frequency, SCL		3.4	MHz
t_{LOW}	Clock Pulse Width Low	160		ns
t_{HIGH}	Clock Pulse Width High	60		ns
t_I [1]	Noise Suppression Time		10	ns
t_{AA}	Clock Low to Data Out Valid	30	160	ns
t_{BUF} [1]	Time the bus must be free before a new transmission can Start	500		ns
$t_{HD.STA}$	Start Hold Time	160		ns
$t_{SU.STA}$	Start Setup Time	160		ns
$t_{HD.DAT}$ [2]	Data In Hold Time	0		ns
$t_{SU.DAT}$	Data In Setup Time	10		ns
t_R	Inputs Rise Time [1]	10	40	ns
t_F	Inputs Fall Time [1]	10	40	ns
$t_{SU.STO}$	Stop Setup Time	160		ns
t_{DH}	Data Out Hold Time	30		ns
t_{WS1}	WP setup time	1		μs
t_{WH1}	WP hold time	1		μs
t_{WS2}	WP release setup time	1		μs
t_{WH2}	WP release hold time	1		μs
t_{WR}	Write Cycle Time		5	ms

Notes: 1. This parameter is characterized and is not 100% tested.

2. As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region of the falling edge of SCL to avoid unintended generation of Start or Stop conditions.

3. AC measurement conditions:

RL (connects to V_{CC}): 330Ω

Input pulse voltages: 0.3 V_{CC} to 0.7 V_{CC}

Input rise and fall times: ≤ 50 ns

Input and output timing reference voltages: 0.5 V_{CC}

Device Operation

CLOCK and DATA TRANSITIONS: The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (refer to Figure 7). Data changes during SCL high periods will indicate a start or stop condition as defined below.

START CONDITION: A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (refer to Figure 8).

STOP CONDITION: A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command will place the EEPROM in a standby power mode (refer to Figure 8).

ACKNOWLEDGE (ACK): All address and data words are serially transmitted to and from the EEPROM in 8-bit words. The EEPROM sends a zero during the ninth clock cycle to acknowledge that it has received each word (refer to Figure 9).

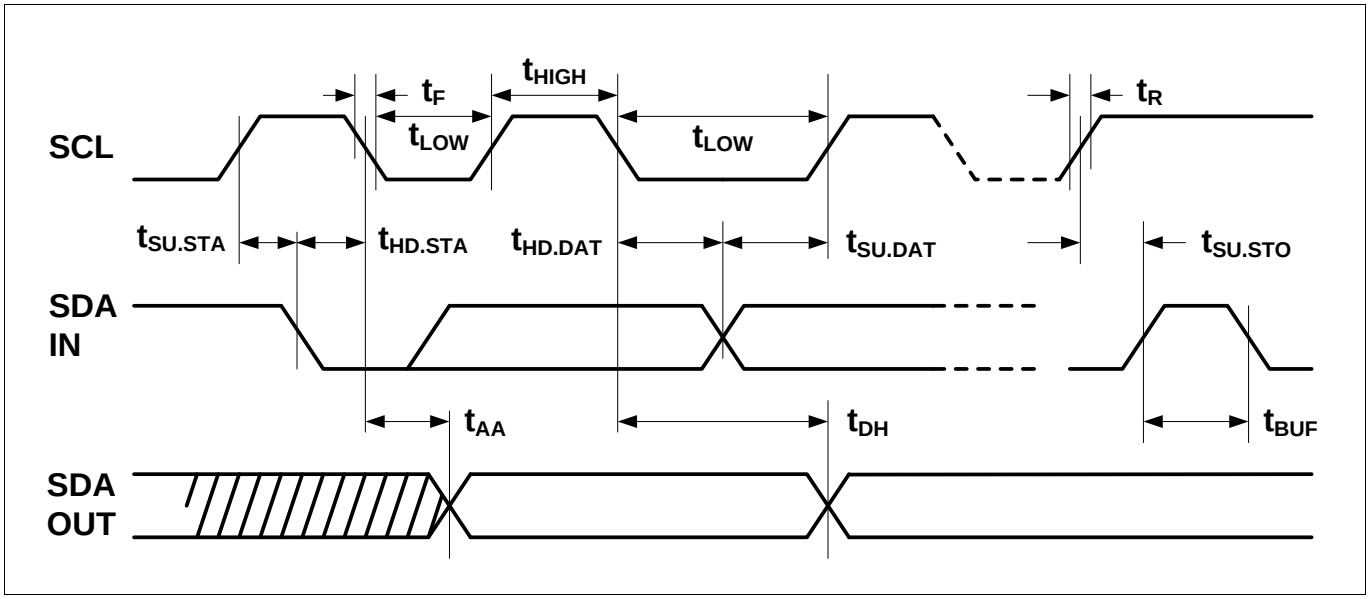
STANDBY MODE: The FM24N256A features a low-power standby mode which is enabled: (a) upon power-up and (b) after the receipt of the stop bit and the completion of any internal operations.

Memory RESET: After an interruption in protocol, power loss or system reset, any 2-wire part can be reset in following these steps:

1. Clock up to 9 Cycles,
2. Look for SDA high in each cycle while SCL is high and then,
3. Create a start condition as SDA is high.

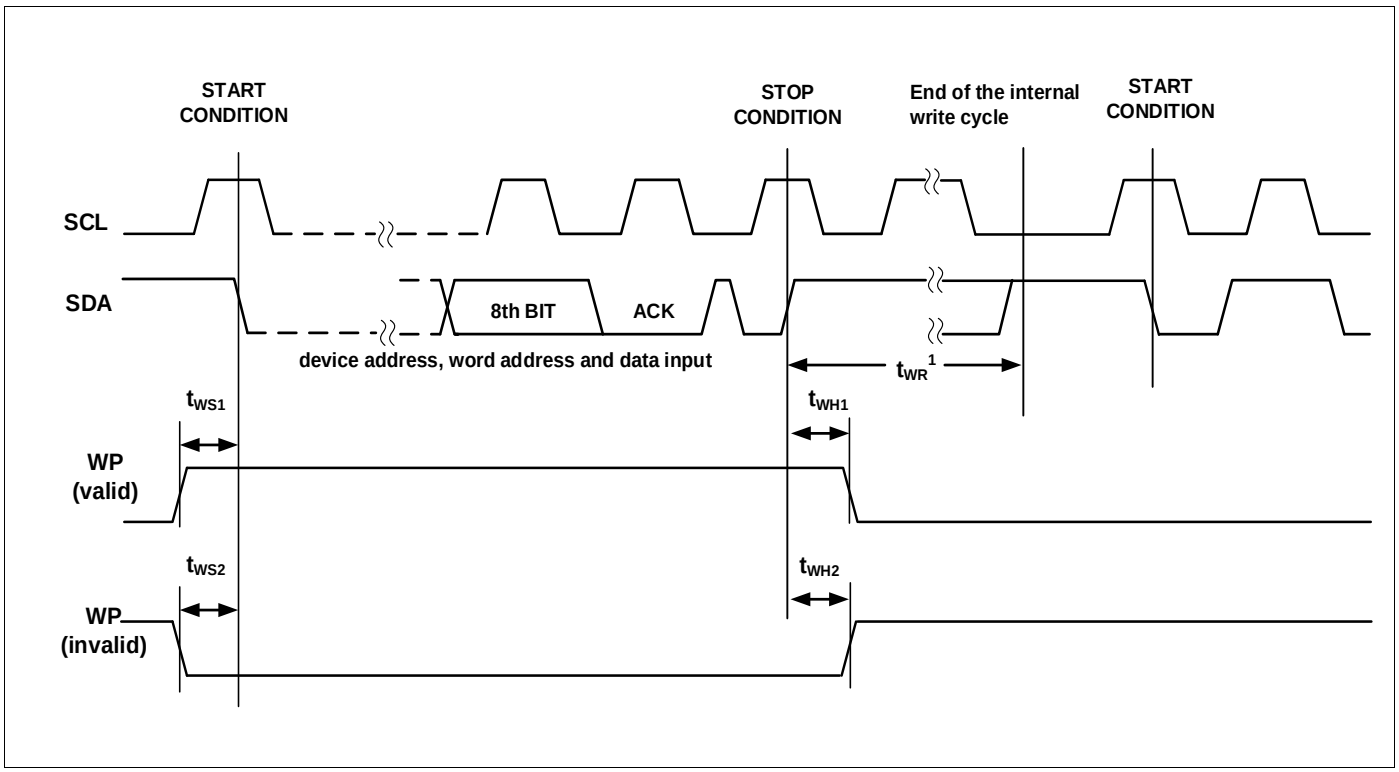
Bus Timing

Figure 5. SCL: Serial Clock, SDA: Serial Data I/O



Write Cycle Timing

Figure 6. SCL: Serial Clock, SDA: Serial Data I/O



Note: 1. The write cycle time t_{WR} is the time from a valid stop condition of a write sequence to the end of the internal clear/write cycle.

Figure 7. Data Validity

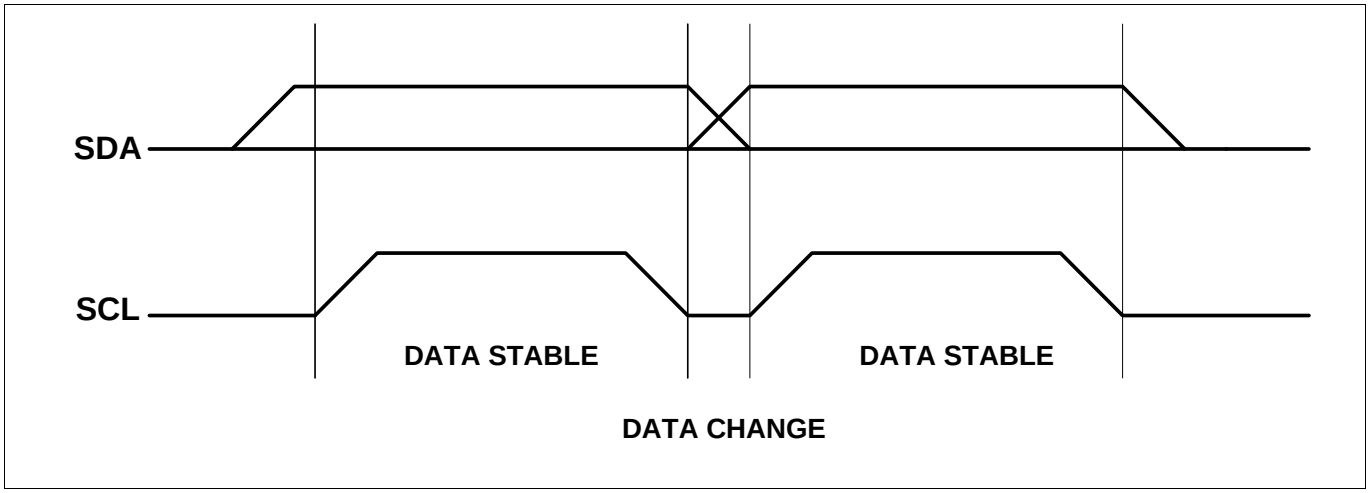


Figure 8. Start and Stop Definition

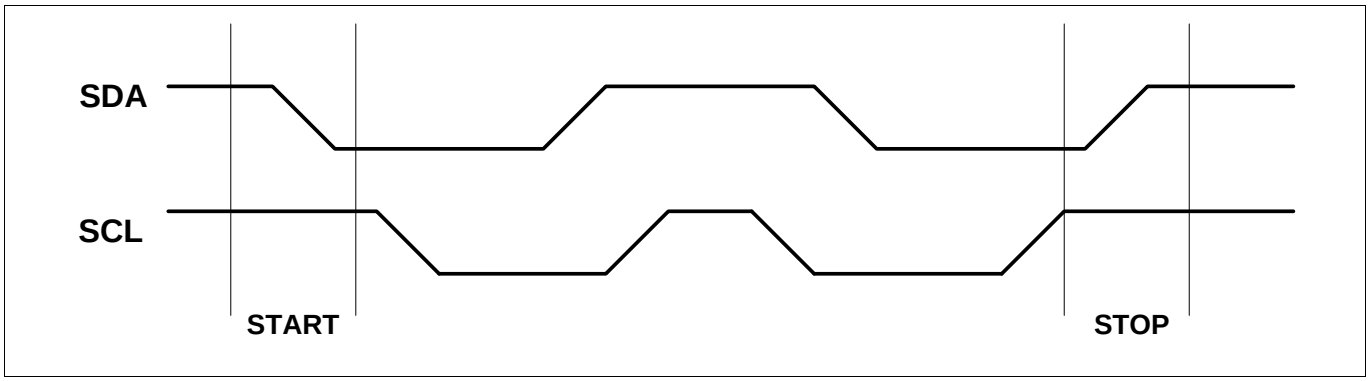
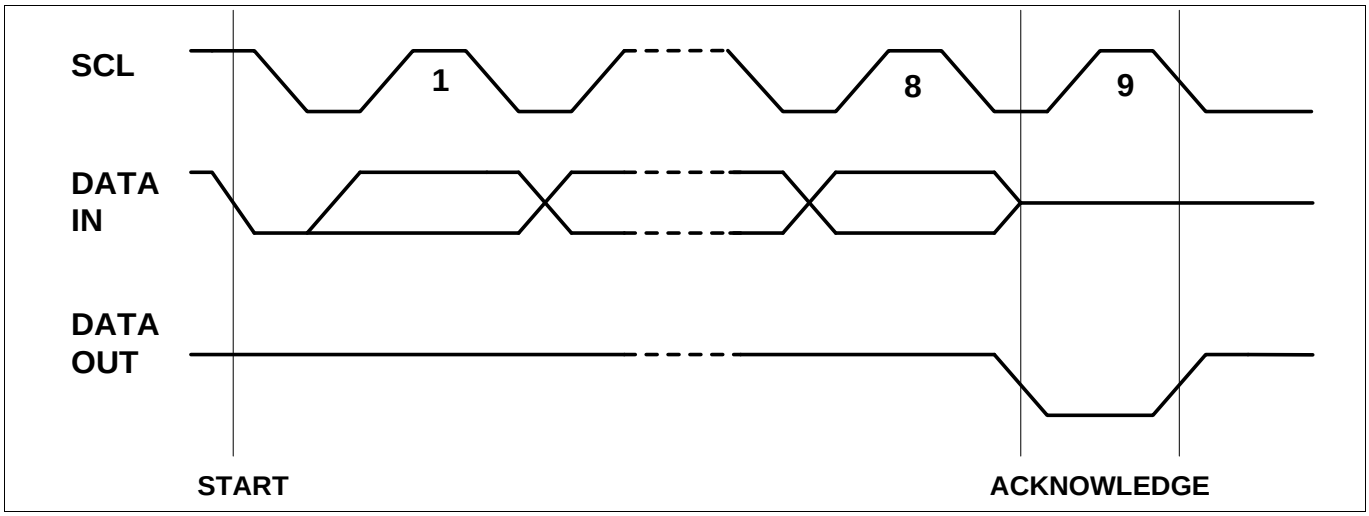


Figure 9. Output Acknowledge



Device Addressing

Data Memory Access: The 256K EEPROM device requires a 8-bit device address word following a start condition to enable the chip for a read or write operation (refer to Table 12).The device address word consists of a mandatory '1010'(Ah) sequence for the first four most significant bits as shown in Table 12. This is common to all the EEPROM devices. The 256K EEPROM uses the three device address bits A2, A1, A0 to allow as many as eight devices on the same bus. These bits must compare to their corresponding hard-wired input pins.

The A2, A1 and A0 pins use an internal proprietary circuit that biases them to a logic low condition if the pins are allowed to float. The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low.

Upon a compare of the device address, the EEPROM will output a zero. If a compare is not made, the device will return to a standby state.

Unique ID Access: The FM24N256A utilizes a separate memory block containing a factory programmed 128-bit unique ID. Access to this memory location is obtained by beginning the device address word with a '1011'(Bh) sequence (refer to Table 12). The behavior of the next three bits (A2, A1 and A0) remains the same as during a standard memory addressing sequence.
The eighth bit of the device address needs be set to a one to read the Serial Number. Writing or altering the 128-bit unique ID is not possible.

For more details on accessing this special feature, See Read Operations on page 20.

Security Sector Access: The FM24N256A offers 64-byte Security Sector which can be written and (later) permanently locked in Read-only mode. Access to this memory location is obtained by beginning the device address word with a '1011'(Bh) sequence (refer to Table 12). The behavior of the next three bits (A2, A1 and A0) remains the same as during a standard memory addressing sequence.

The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low.

For more details on accessing this special feature, See Write Operations and Read Operations on page 19,20.

ECC Error Status Register Access: The FM24N256A offers 1-bit ECC Error Status Register (EESR) to indicate whether there is a single error bit in a group of four bytes during a Read operation. Access to EESR is obtained by beginning the device address word with a '1011'(Bh) sequence (refer to Table 12~Table 14). The behavior of the next three bits (A2, A1 and A0) remains the same as during a standard memory addressing sequence. The eighth bit of the device address needs be set to a one to read the EESR.

For more details on accessing this special feature, See Read Operations on page 20.

NOISE PROTECTION: Special internal circuitry placed on the SDA and SCL pins prevent small noise spikes from activating the device.

DATA SECURITY: The Device has a hardware data protection scheme that allows the user to write protect the entire memory when the WP pin is at V_{CC}.

Table 12. Device Address

Access Area	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Data Memory	1	0	1	0	A2	A1	A0	R/W
Security Sector	1	0	1	1	A2	A1	A0	R/W
Security Sector Lock Bit	1	0	1	1	A2	A1	A0	R/W
Unique ID Number	1	0	1	1	A2	A1	A0	1
EESR	1	0	1	1	A2	A1	A0	1
	MSB							LSB

Table 13. First Word Address

Access Area	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Data Memory	x	A14	A13	A12	A11	A10	A9	A8
Security Sector	x	x	x	x	x	0	0	x
Security Sector Lock Bit	x	x	x	x	x	1	0	X
Unique ID Number	x	x	x	x	x	0	1	x
EESR	0	0	0	0	0	1	1	0
	MSB							LSB

NOTE: x = Don`t care bit.

Table 14. Second Word Address

Access Area	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Data Memory	A7	A6	A5	A4	A3	A2	A1	A0
Security Sector	x	A6	A5	A4	A3	A2	A1	A0
Security Sector Lock Bit	x	x	x	x	x	x	x	x
Unique ID Number	x	x	x	x	0	0	0	0
EESR	0	0	0	0	0	1	0	1
	MSB							LSB

NOTE: x = Don`t care bit.

Write Operations

BYTE WRITE: A write operation requires two 8-bit data word address following the device address word and acknowledgment. Upon receipt of this address, the EEPROM will again respond with a zero and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will output a zero and the addressing device, such as a microcontroller, must terminate the write sequence with a stop condition. At this time the EEPROM enters an internally-timed write cycle, t_{WR}, to the nonvolatile memory. All inputs are disabled during this write cycle and the EEPROM will not respond until the write is complete (see Figure 11).

PAGE WRITE: The 256K EEPROM is capable of 64-byte page writes. A page write is initiated the same way as a byte write, but the microcontroller does not send a stop condition after the first data word is clocked in. Instead, after the EEPROM acknowledges receipt of the first data word, the microcontroller can transmit up to 63 more data words. The EEPROM will respond with a zero after each data word received. The microcontroller must terminate the page write sequence with a stop condition (see Figure 12).

The data word address lower seven bits are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than 64 data words are transmitted to the EEPROM, the data word address will “roll over” and previous data will be overwritten.

ACKNOWLEDGE POLLING: Once the internally timed write cycle has started and the EEPROM inputs are disabled, acknowledge polling can be initiated. This involves sending a start condition followed by the device address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has completed will the EEPROM respond with a zero allowing the read or write sequence to continue (see Figure 10).

WRITE SECURITY SECTOR: Write the Security Sector is similar to the page write but requires use of device address, and the special word address seen in Table 12 . The higher address bits ADDR<15:7> are don’t care except for address bits ADDR<10:9>，which must be equal to ‘00b’. Lower address bits ADDR<5:0> define the byte address inside the Security Sector (see Figure 18).

If the Security Sector is locked, the data bytes transferred during the Write Security Sector operation are not acknowledged (NoACK).

LOCK SECURITY SECTOR: Lock the Security Sector is similar to the byte write but requires use of device address, and special word address seen in Table 12 . The word address bits ADDR<10:9> must be ‘10b’, all other word address bits are don’t care. The data byte must be equal to the binary value xxxx xx1x, where x is don't care (see Figure 20).

If the Security Sector is locked, the data bytes transferred during the Lock Security Sector operation are not acknowledged (NoACK).

Cycling with Error Correction Code (ECC):

The FM24N256A offer an Error Correction Code (ECC) logic. The ECC is an internal logic function which is transparent for the 2-wire Serial communication protocol. The ECC logic is implemented on each group(1) of four EEPROM bytes. Inside a group, if a single bit out of the four bytes happens to be erroneous during a Read operation, the ECC detects this bit and replaces it with the correct value. The read reliability is therefore much improved. Even if the ECC function is performed on groups of four bytes, a single byte can be written/cycled independently. In this case, the ECC function also writes/cycles the three other bytes located in the same group(1). As a consequence, the maximum cycling budget is defined at group level and the cycling can be distributed over the four bytes of the group: the sum of the cycles seen by byte0, byte1, byte2 and byte3 of the same group must remain below the maximum value defined in Section Cycling Performance By Groups Of Four Bytes on Page 10.

Note：

1. A group of four bytes is located at addresses [4*N, 4*N+1, 4*N+2, 4*N+3], where N is an integer.

Read Operations

Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to one.

CURRENT ADDRESS READ: The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address "roll over" during read is from the last byte of the last memory page to the first byte of the first page. The address "roll over" during write is from the last byte of the current page to the first byte of the same page.

Once the device address with the read/write select bit set to one is clocked in and acknowledged by the EEPROM, the current address data word is serially clocked out. The microcontroller does not respond with an input zero but does generate a following stop condition (see Figure 15).

RANDOM READ: A random read requires a "dummy" byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the EEPROM, the microcontroller must generate another start condition. The microcontroller now initiates a current address read by sending a device address with the read/write select bit high. The EEPROM acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a zero but does generate a following stop condition (see Figure 16).

SEQUENTIAL READ: Sequential reads are initiated by either a current address read or a random address read. After the microcontroller receives a data word, it responds with an acknowledge. As long as the EEPROM receives an acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will "roll over" and the sequential read will continue. The sequential read operation is terminated when the microcontroller does not respond with a zero but does generate a following stop condition (see Figure 17)

UNIQUE ID READ: Reading the serial number is similar to the sequential read but requires use of the device address, a dummy write, and the use of specific word address seen in Table 12 . The higher address bits ADDR<15:4> are don't care except for address bits ADDR<10:9>，which must be equal to '01b'. Lower address bits ADDR<3:0> define the byte address inside the UID. If the application desires to read the first byte of the UID, the lower address bits ADDR<3:0> would need to be '0000b'.

When the end of the 128-bit UID number is reached (16 bytes of data), the data word address will roll-over back to the beginning of the 128-bit UID number. The Unique ID Read operation is terminated when the microcontroller does not respond with a zero (NoACK) and instead issues a Stop condition (see Figure 22).

READ SECURITY SECTOR：Read the Security Sector is similar to the random read but requires use of device address, a dummy write, and the use of specific word address seen in Table 12 . The higher address bits ADDR<15:7> are don't care except for address bits ADDR<10:9>， which must be equal to '00b'. The lower address bits ADDR<5:0> define the byte address inside the Security Sector.

The internal byte address is automatically incremented to the next byte address after each byte of data is clocked out. When the last byte (3Fh) is reached, it will roll over to 00h, the first byte of the Security Sector, and continue to increment (see Figure 19).

READ LOCK STATUS：There are two ways to check the lock status of the Security Sector.
1. The first way is initiated by a Security Sector Write, the EEPROM will acknowledge if the Security Sector is unlocked, while it will not acknowledge if the Security Sector is locked.
Once the acknowledge bit is read, it is recommended to generate a Start condition followed by a Stop condition, so that:

- Start: the truncated command is not executed because the Start condition resets the device internal logic
- Stop: the device is then set back into Standby mode by the Stop condition.

2. The second way is initiated by a Lock Status Read. Lock Status Read is similar to the random read but requires use of device address seen in Table 12 , a dummy write, and the use of specific word address. The address bits ADDR<10:9> must be '10b', all other address bits are Don't Care. The Lock bit is the BIT1 of the byte read on SDA. It is at "1" when the lock is active and at "0" when the lock is not active. The same data is shifted out repeatedly until

the microcontroller does not respond with a zero but does generate a following stop condition (see Figure 21).

READ ECC ERROR STATUS REGISTER: The microcontroller cannot detect a single error bit issue during a Read operation because the ECC is an internal logic function that remains transparent to the 2-wire Serial communication protocol. To identify error bits after a Read operation, the device provides a 1-bit volatile and read only ECC Error Status Register (EESR). Reading the EESR bit is similar to random read, but it necessitates the use of device address from Table 11 to Table 13, a dummy write, and the specific word address. The hex value for the address bits ADDR<15:0> needs to be configured to 0x0605h. The EESR is indicated by the full byte read on SDA. It reads as 0x80h when one or more error bits are present and as 0x00h when the group of four bytes is completely accurate. The data is shifted repeatedly until the microcontroller responds with a non-zero value followed by a stop condition (refer to
Figure **23**).
If the users want to find the group address contains the error bit, according to the following steps:

- Start reading from the address of the user concerned. The Read operation must by group address, and then following the Read EESR operation. If current group address is no error, then reading the next group address.
- Reading by group address and Read EESR operation must be executed alternately until the error group address is found.
- The EESR bit will be set to logic ‘0b’ unless the previously executed read operation required the use of the ECC logic scheme. When this occurs, the EESR bit will set to logic ‘1’. The EESR bit will continue to read a logic ‘1’ until another read operation is issued and the use of the ECC logic scheme was not required or a Power-on Reset (POR) event occurred.

Figure 10. ACKNOWLEDGE POLLING

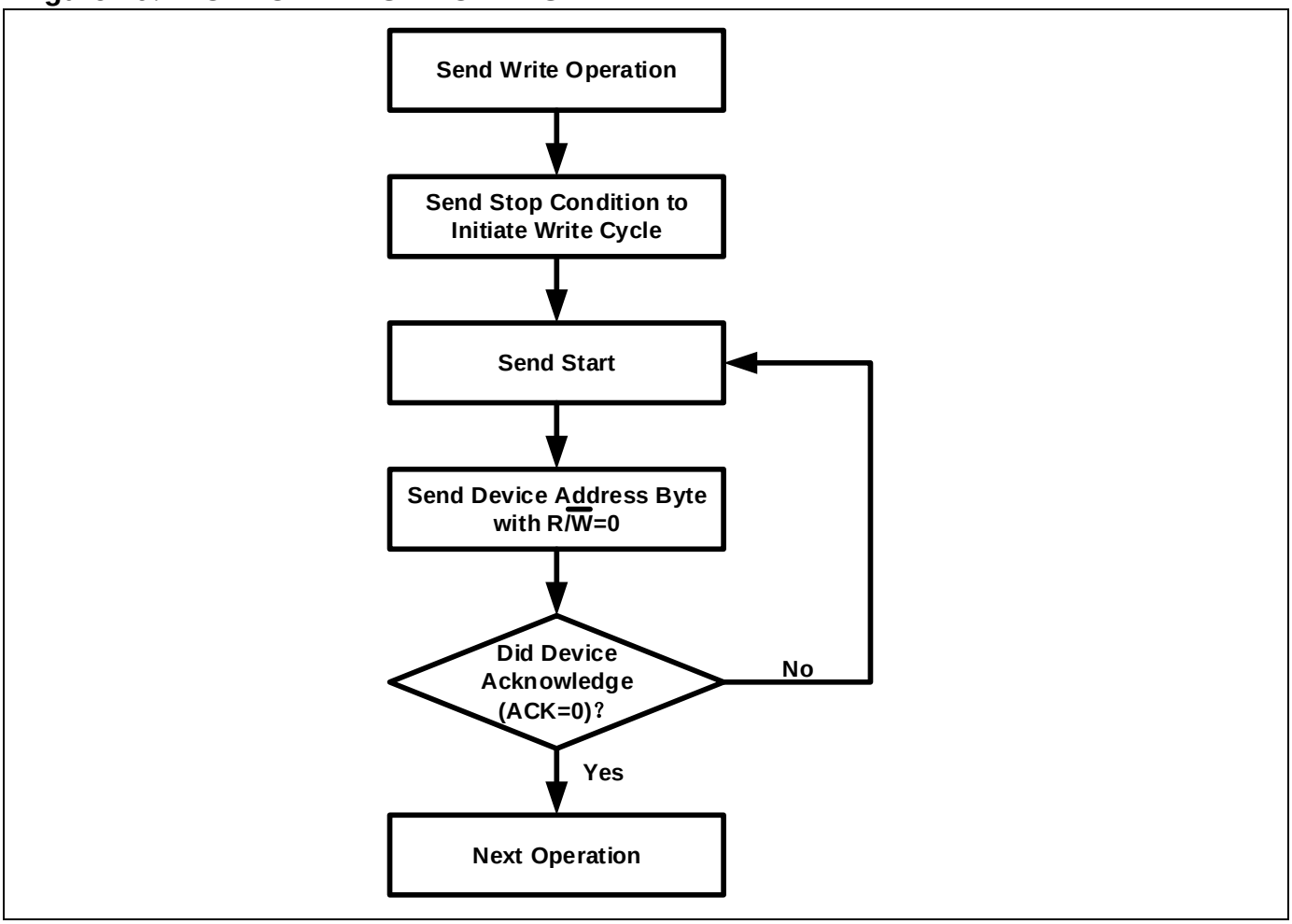
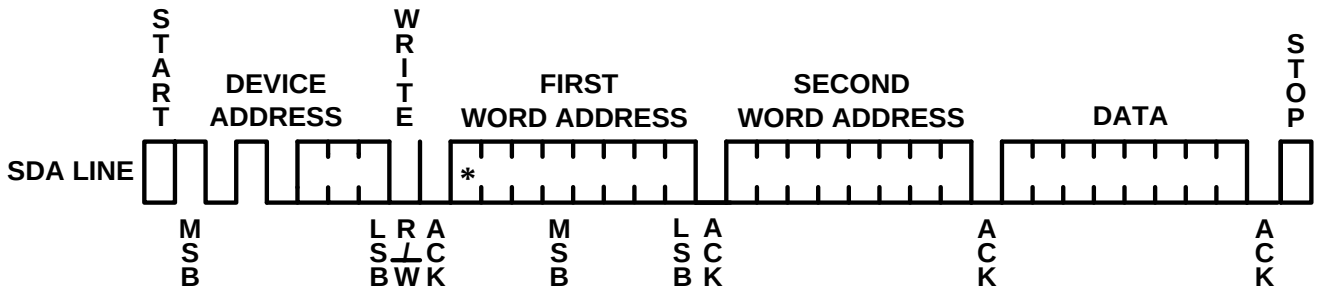
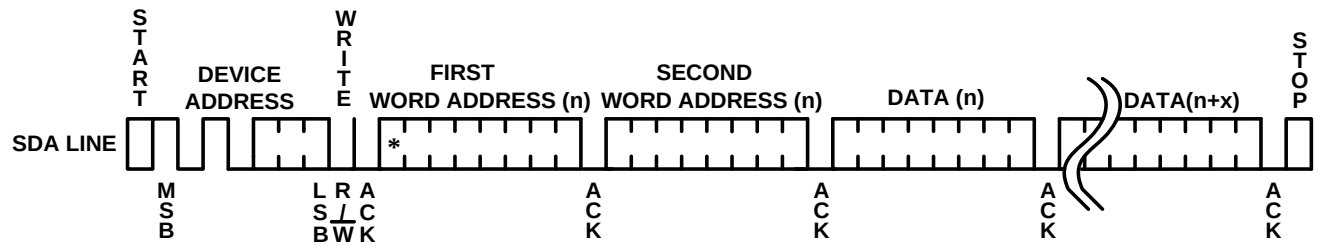


Figure 11. Byte Write



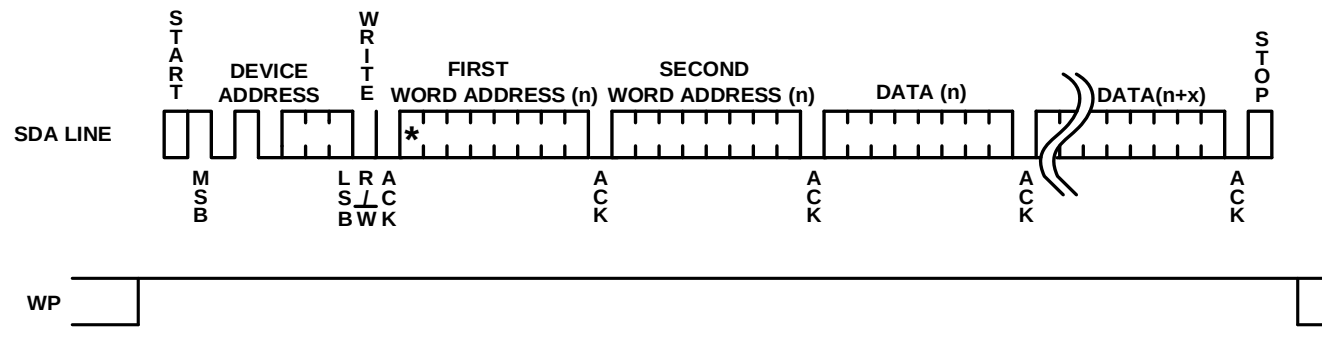
Note: 1. * = *Don't CARE* bits

Figure 12. Page Write



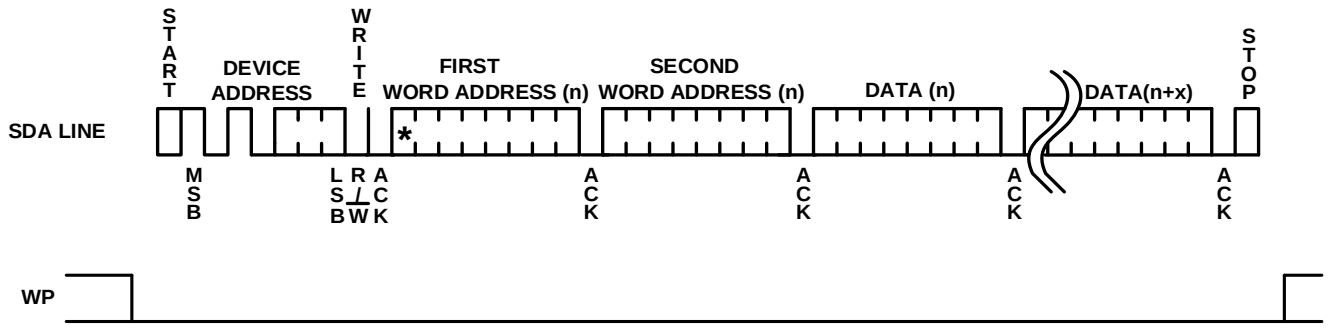
Note: 1. * = *Don't CARE* bits

Figure 13. Write-Protect Condition



Note: 1. * = *Don't CARE* bits

Figure 14. Non-Write-Protect Condition



Note: 1. * = *Don't CARE* bits

Figure 15. Current Address Read

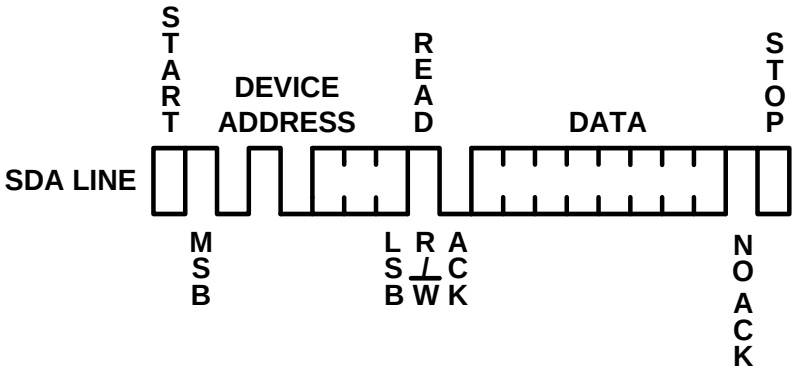
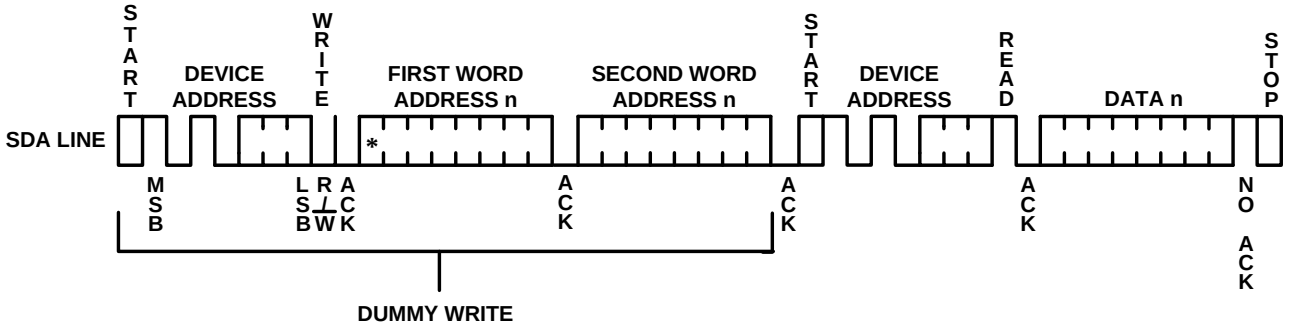


Figure 16. Random Read



Note: 1. * = *Don't CARE* bits.

Figure 17. Sequential Read

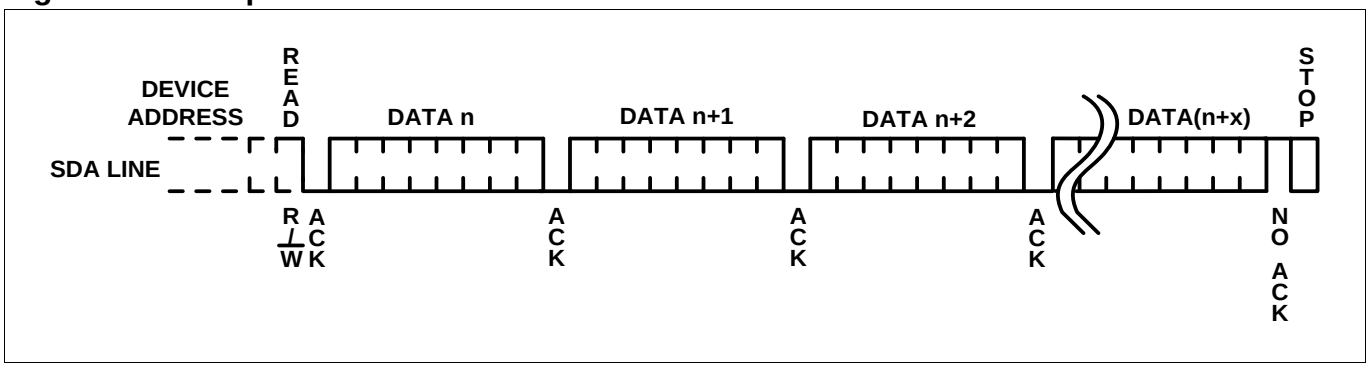
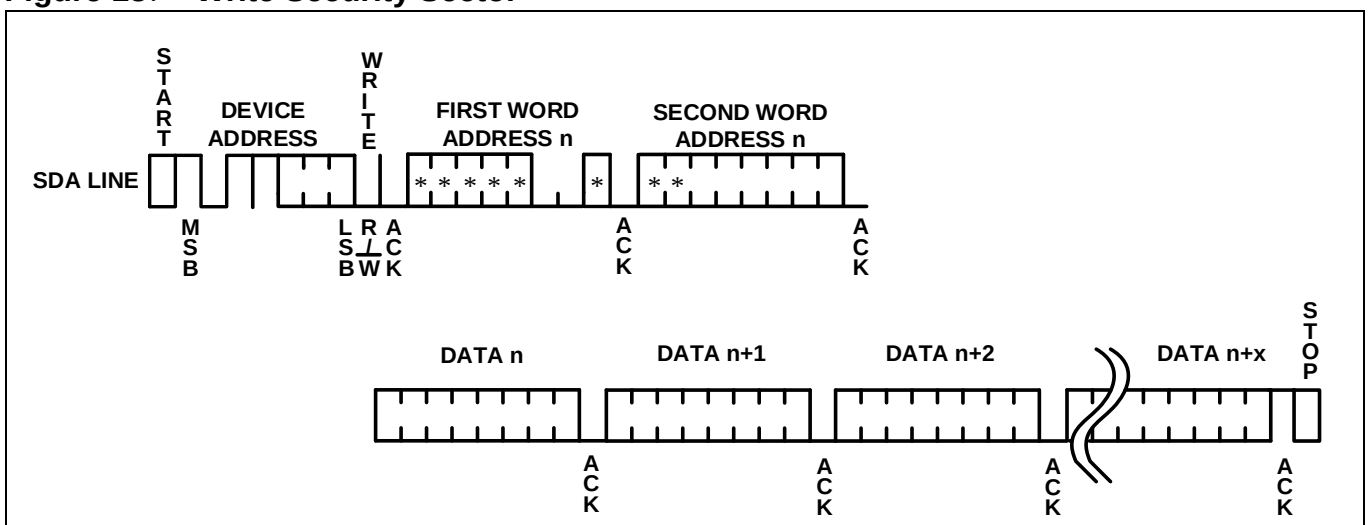
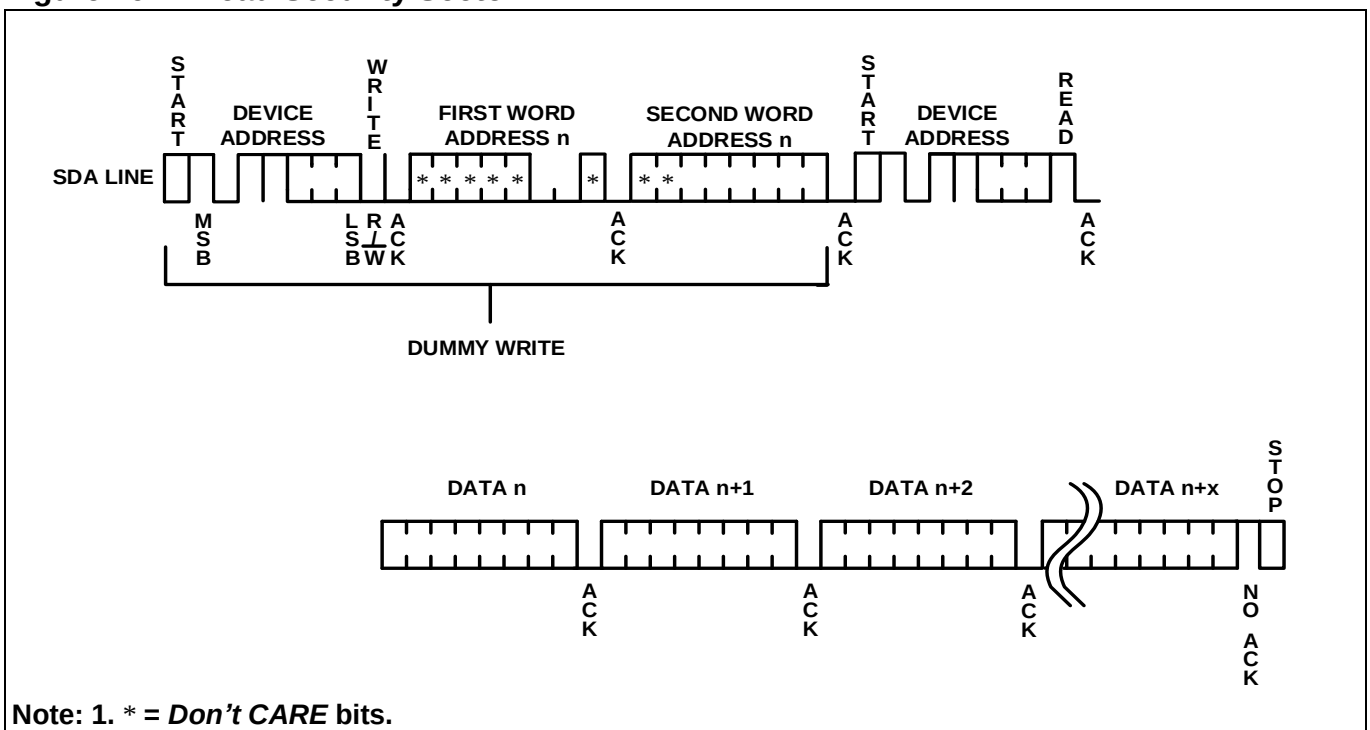


Figure 18. Write Security Sector



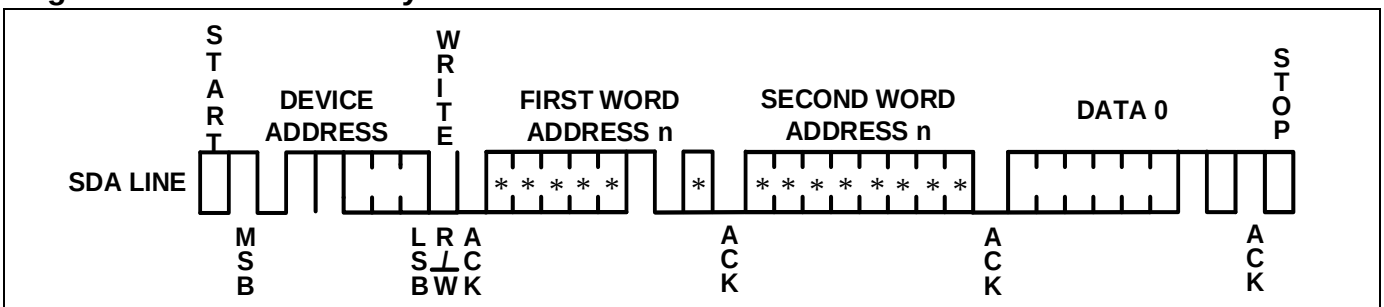
Note: 1. * = *Don't CARE* bits.

Figure 19. Read Security Sector



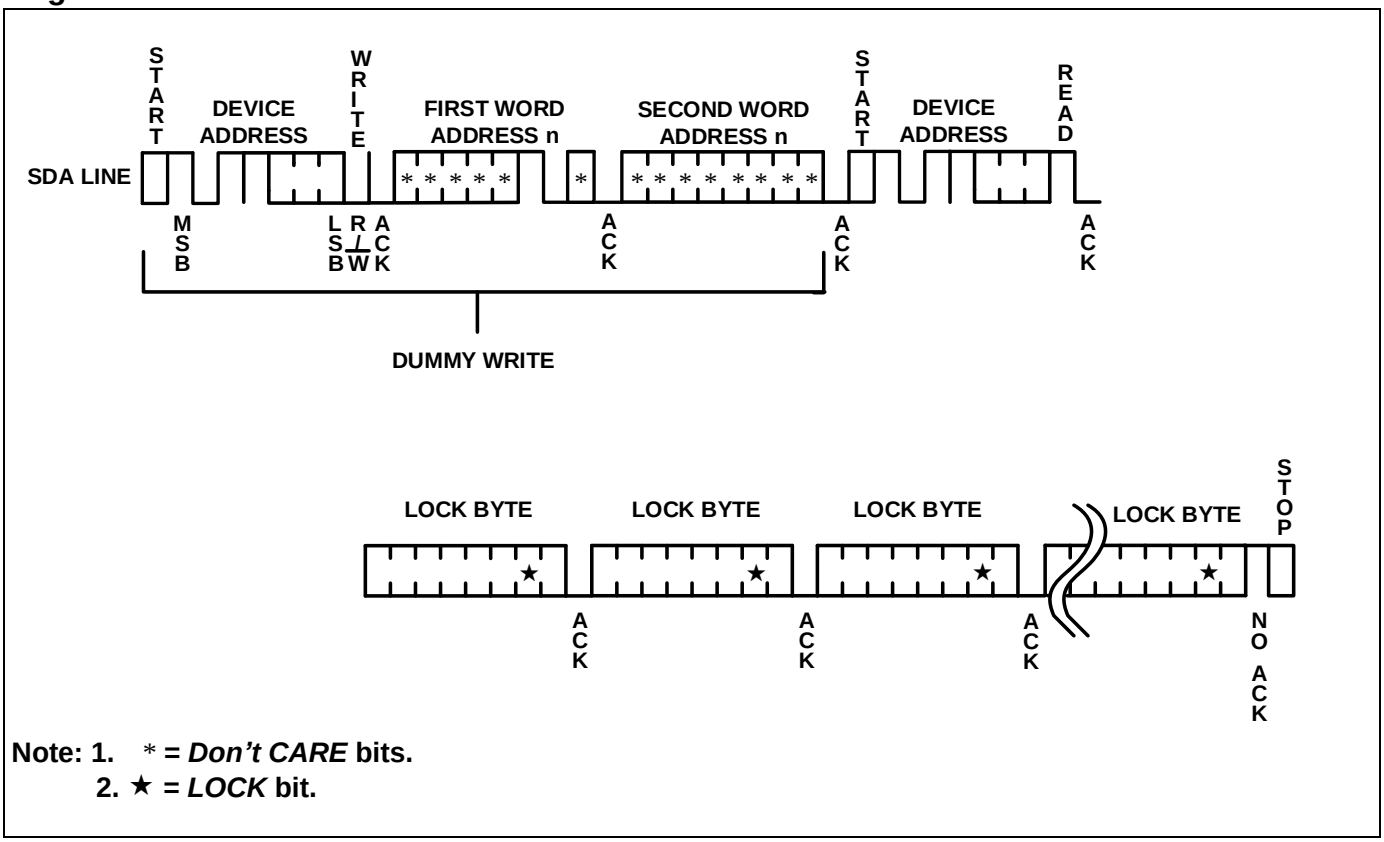
Note: 1. * = *Don't CARE* bits.

Figure 20. Lock Security Sector



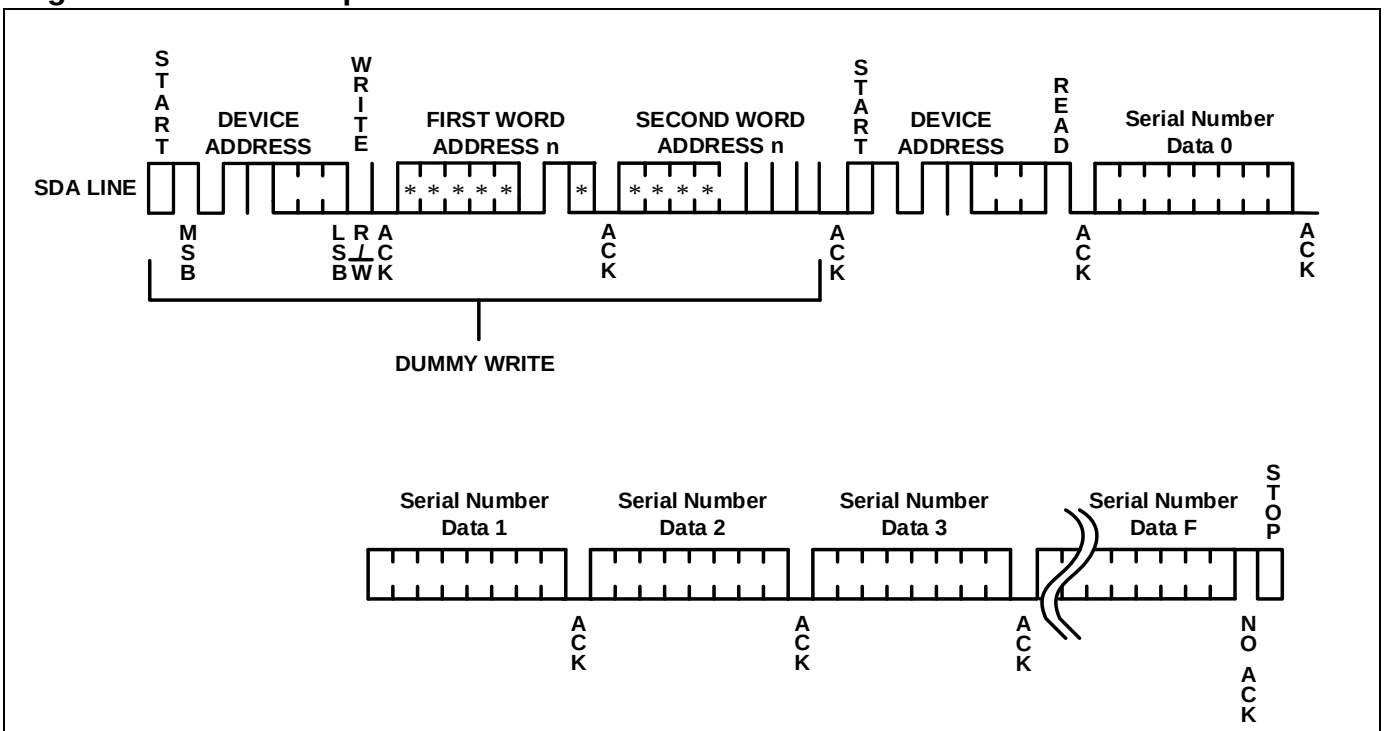
Note: 1. * = *Don't CARE* bits.

Figure 21. Read Lock Status



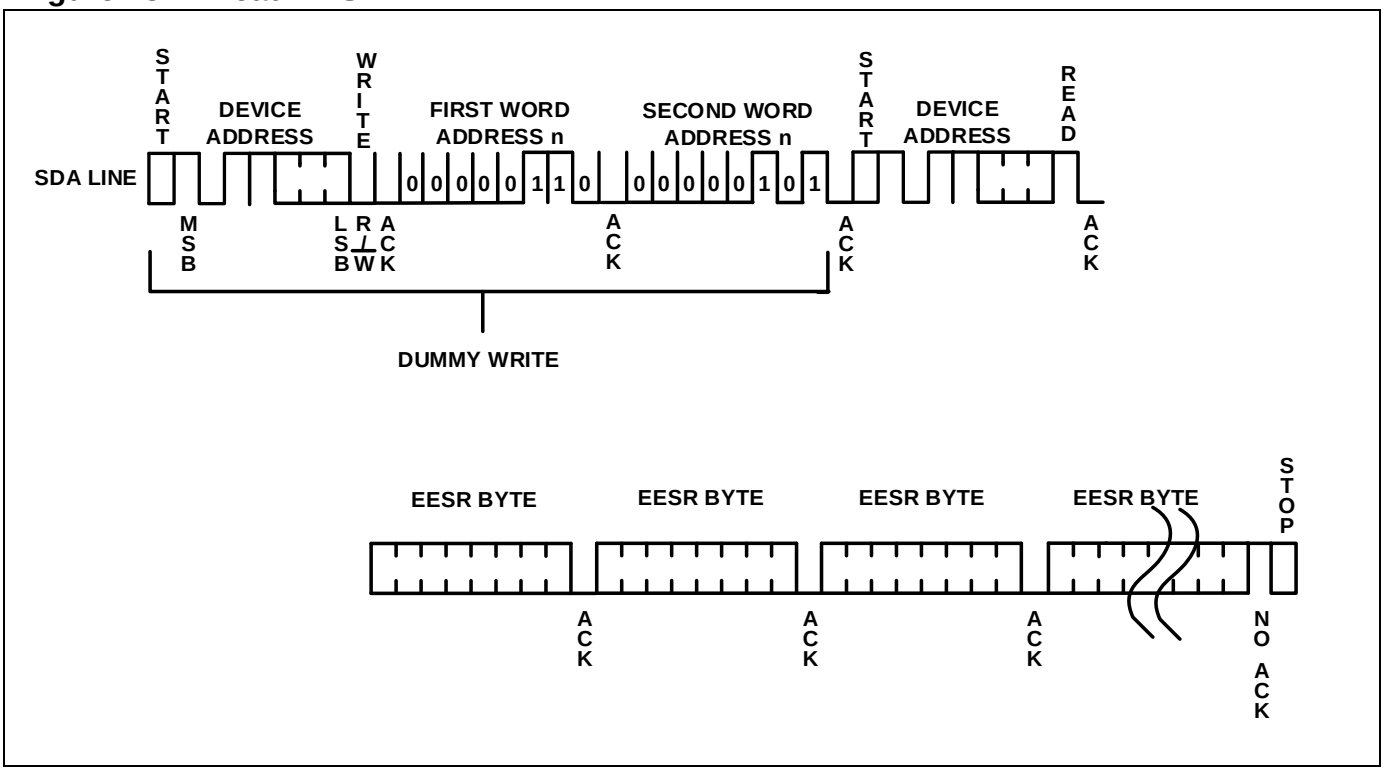
Note: 1. * = *Don't CARE* bits.
2. ★ = *LOCK* bit.

Figure 22. Read Unique ID

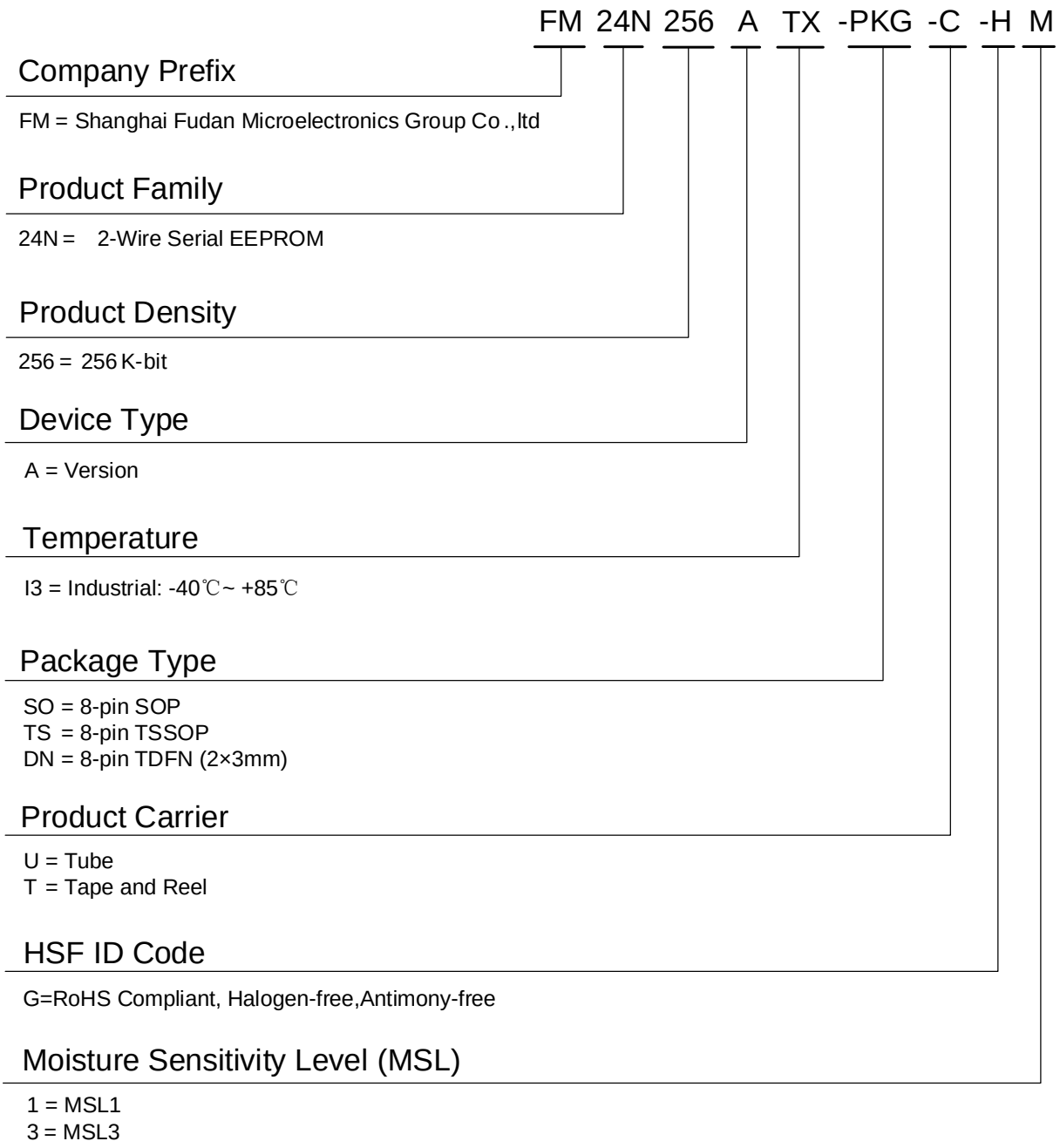


Note: 1. * = *Don't CARE* bits.

Figure 23. Read EESR



Ordering Information

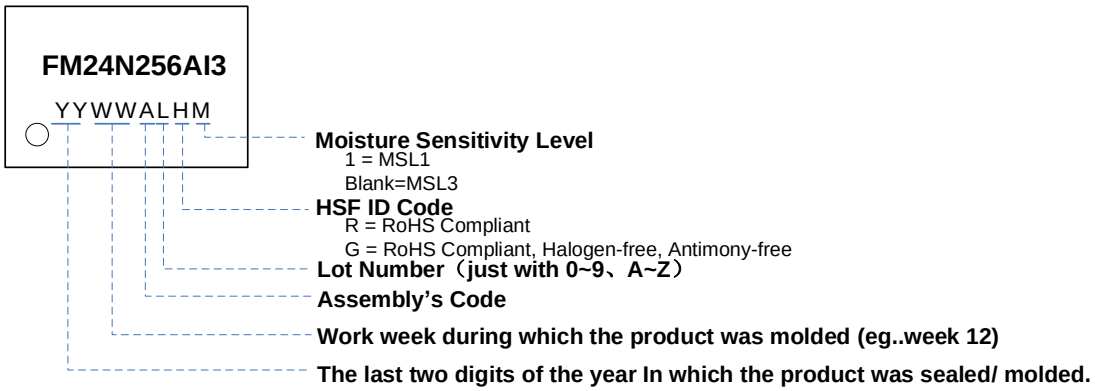


Note:

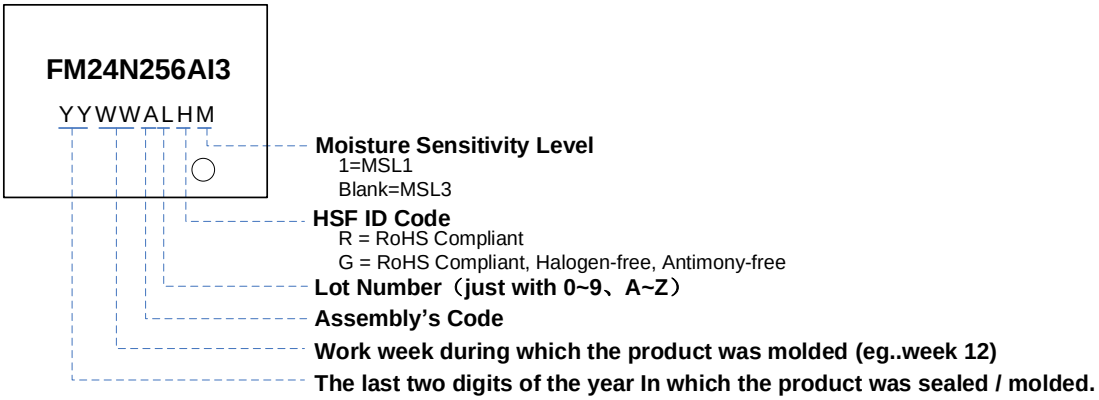
1. For Thinner package please contact local sales office.
2. For SO, TS and DN package: G class only.

Part Marking Scheme

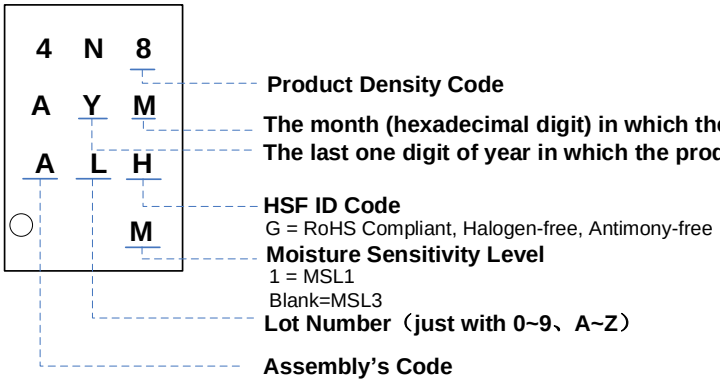
SOP8



TSSOP8



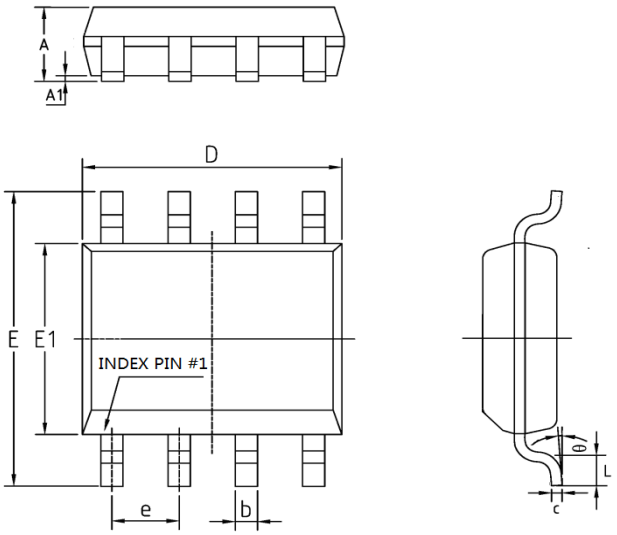
TDFN8



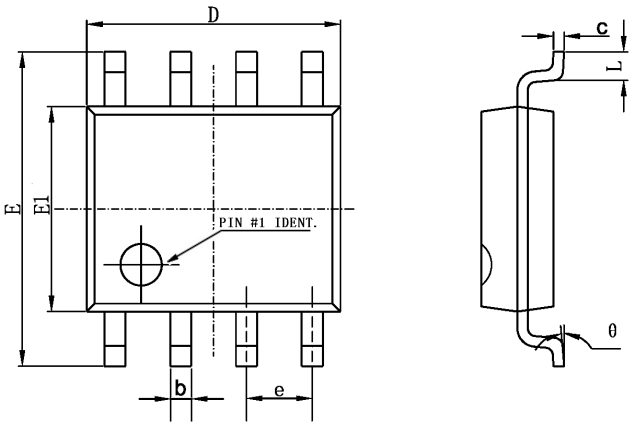
Packaging Information

SOP 8

(1)



(2)

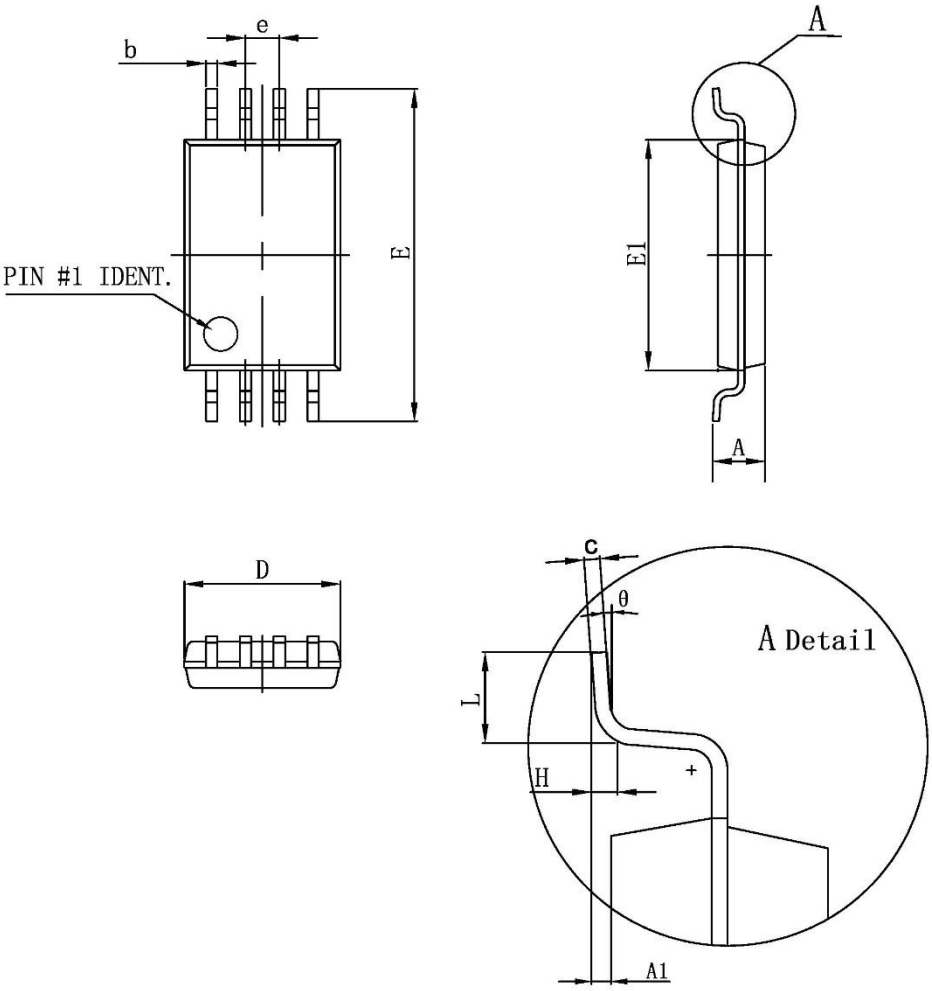


Symbol	MIN	MAX
A	1.350	1.750
A1	0.050	0.250
b	0.330	0.510
c	0.150	0.250
D	4.700	5.150
E1	3.700	4.100
E	5.800	6.200
e	1.270(BSC)	
L	0.400	0.900
θ	0°	8°

NOTE:

1. **Dimensions are in Millimeters.**

TSSOP8

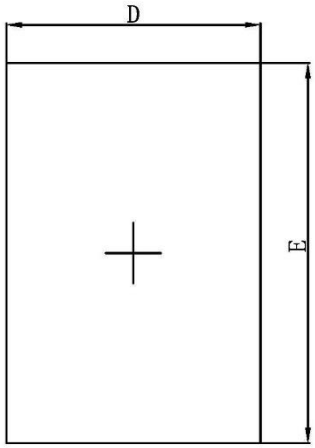


Symbol	MI	MAX
D	2.900	3.100
E1	4.300	4.500
b	0.190	0.300
c	0.090	0.200
E	6.200	6.600
A		1.200
A1	0.050	0.150
e	0.650 (BSC)	
L	0.450	0.750
θ	0°	8°

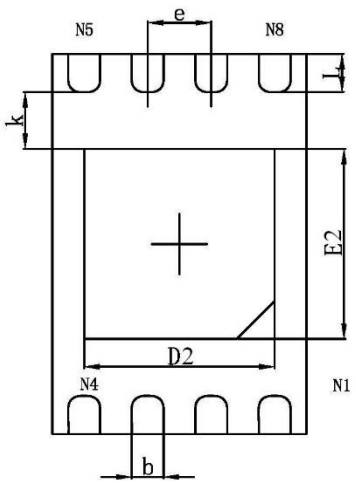
NOTE:

1. Dimensions are in Millimeters.

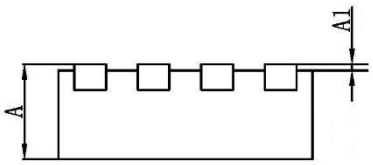
TDFN8(2x3mm)



Top View



Bottom View



Side View

Symbol	MIN	MAX
A	0.700	0.800
A1	0.000	0.050
D	1.900	2.100
E	2.900	3.100
D2	1.400	1.600
E2	1.400	1.700
k	0.150(MIN)	
b	0.180	0.300
e	0.500(TYP)	
L	0.200	0.500

NOTE:

1. **Dimensions are in Millimeters.**

Revision History

Version	Publication date	Pages	Revise Description
1.0	Nov. 2023	34	Initial document Release.
1.1	Jan. 2024	34	1. Correct the typo. 2. Updated “Table 4. High-Speed Mode Host Code”
1.2	Jan. 2025	34	1. Updated the chapters of Write Protect Description.

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