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FM25S02BI3

3.3V 2G-BIT SPI NAND FLASH MEMORY

Datasheet

Apr. 2024

Trademarks

1. Description

The FM25S02BI3 is a 2G-bit (256M-byte) SPI (Serial Peripheral Interface) NAND Flash memory, with advanced write protection mechanisms. The FM25S02BI3 supports the standard Serial Peripheral Interface (SPI), Dual/Quad I/O option.

2. Features

- **2G bitNAND Flash Memory**
  - Single-level cell (SLC) technology
  - Page size : 2176 bytes(2048 + 128 bytes)
  - Block size : 64 pages(128K + 8K bytes)
  - Device size: 2Gb(2048 blocks)
- **Serial Interface**
  - Standard SPI: CLK, CS#, DI, DO, WP#
  - Dual SPI: CLK, CS#, DQ0, DQ1, WP#
  - Quad SPI: CLK, CS#, DQ0, DQ1, DQ2, DQ3
- **High Performance**
  - 104MHzfor fast read
  - Quad I/O data transfer up to 416Mbits/s
- **Wide Range Supply Voltage**
  - FM25S02BI3 :2.7V~3.6V
- **Low Power, Wide Temperature Range**
  - 20mA active current
  - -40~85°C operating range
- **Program/Erase/Read Speed**
  - PAGE PROGRAM time : 400μs typical
  - BLOCK ERASE time : 4ms typical
  - PAGE READ time :
    70μs maximum(with ECC)
    25μs maximum(without ECC)
- **Advanced Features for NAND**
  - 8bit Internal ECC option, per 528 bytes
  - Software and Hardware Write-Protect
  - 32B Unique ID and 2KB parameter page
  - 25 OTP pages
  - INTERNAL DATA MOVE by page
  - Promised golden block0
- **Package**
  - WSON8 8x6mm (TDFN8 8x6mm)
  - BGA24 8x6mm 5*5 Ball Array
  - BGA24A 8x6mm 4*6 Ball Array
  - All Packages are RoHS Compliant and Halogen-free
- **Minimum 60,000 Program/Erase Cycles**
- **Data Retention: 10 years**

3. Packaging Type and Pin Configurations

FM25S02BI3 is offered inWSON8 8x6mm (TDFN8 8x6mm) and BGA24 packages as shown in Figure 1 Pad Assignments,

WSON8 8x6mm TDFN8 (8x6mm)

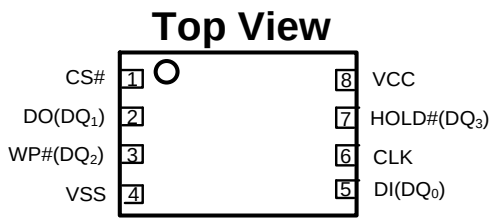
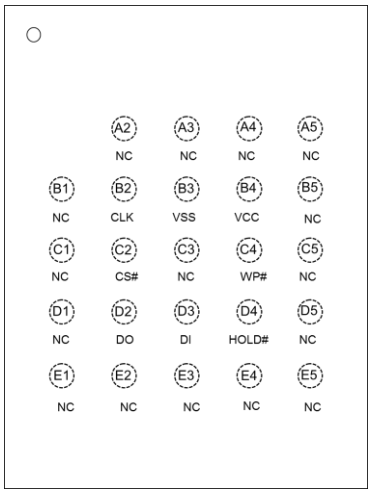
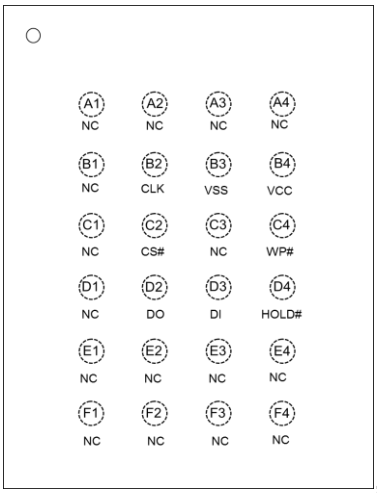


Figure 2 Pad Assignments

BGA24 8x6mm 5*5 Ball Array



BGA24A 8x6mm 4*6 Ball Array



, and Figure 2 respectively. Package diagrams and dimensions are illustrated at the end of this datasheet.

Figure 1 Pad Assignments,

WSON8 8x6mm TDFN8 (8x6mm)

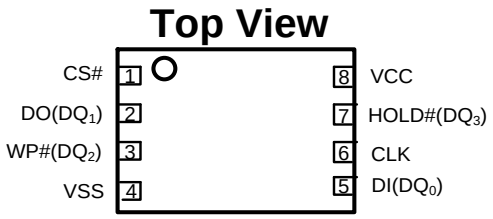
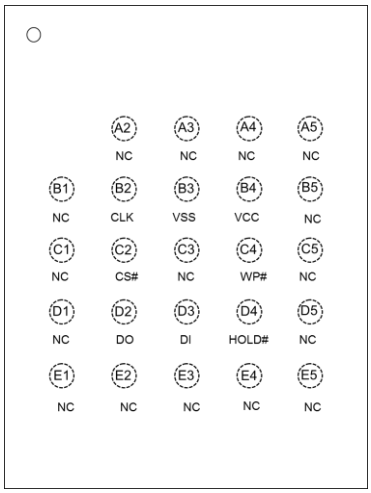
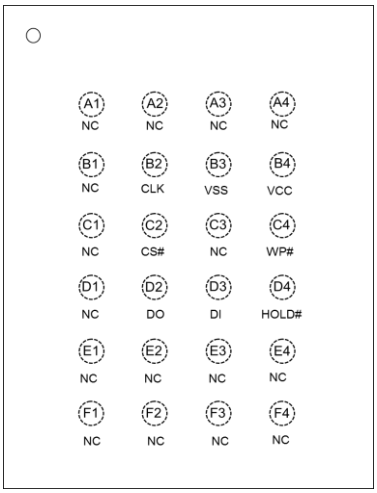


Figure 2 Pad Assignments

BGA24 8x6mm 5*5 Ball Array



BGA24A 8x6mm 4*6 Ball Array



3.1. Pin Description

Table 1 Pin Description

PIN NO.	PIN NAME	I/O	FUNCTION
1	CS#	I	Chip Select Input
2	DO (DQ_1)	I/O	Data Output (Data Input Output 1)(1)
3	WP# (DQ_2)	I/O	Write Protect Input (Data Input Output 2)(2)

4	VSS		Ground
5	DI (DQ_0)	I/O	Data Input (Data Input Output 0)(1)
6	CLK	I	Serial Clock Input
7	HOLD# (DQ_3)	I/O	Hold Input (Data Input Output 3)(2)
8	VCC		Power Supply

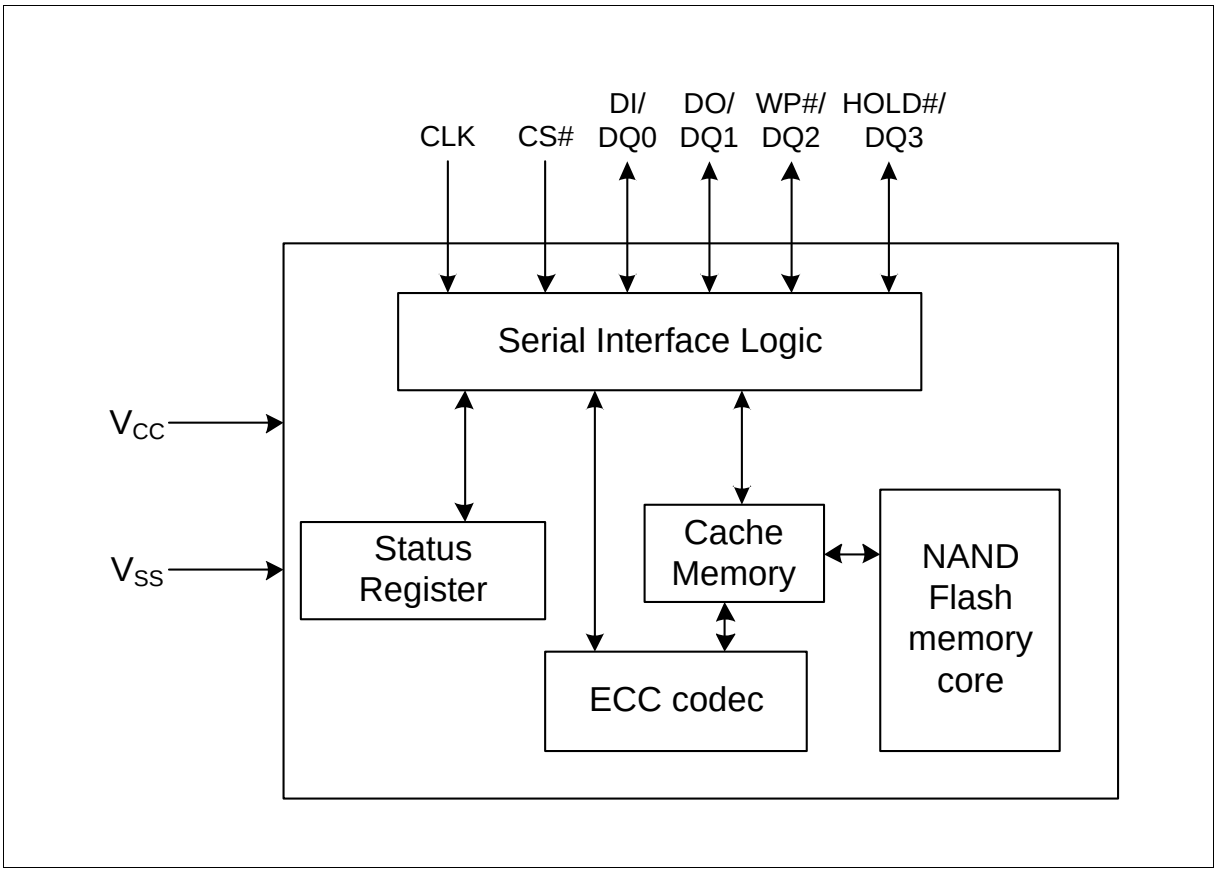
Notes:

1 DQ_0 and DQ_1 are used for Dual SPI instructions.

2 DQ_0- DQ_3 are used for Quad SPI instructions.

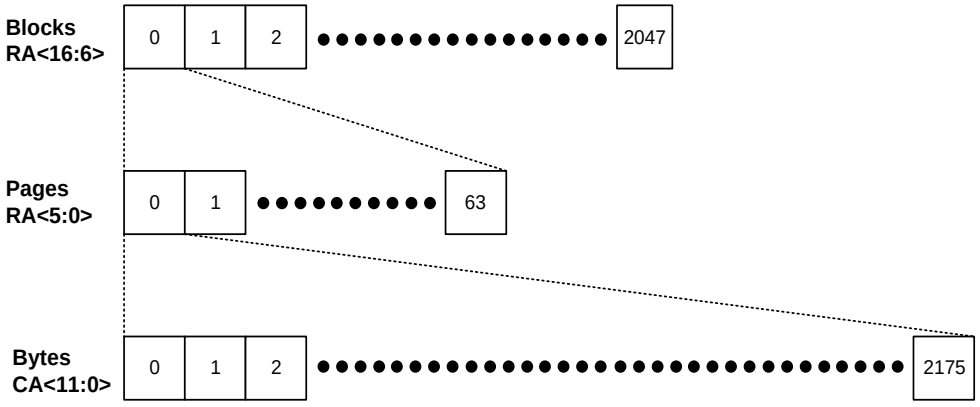
4. Block Diagram

Figure 2 SPI NAND Flash Memory Block Diagram



5. Memory Mapping

Figure 3 Memory Map



Note:

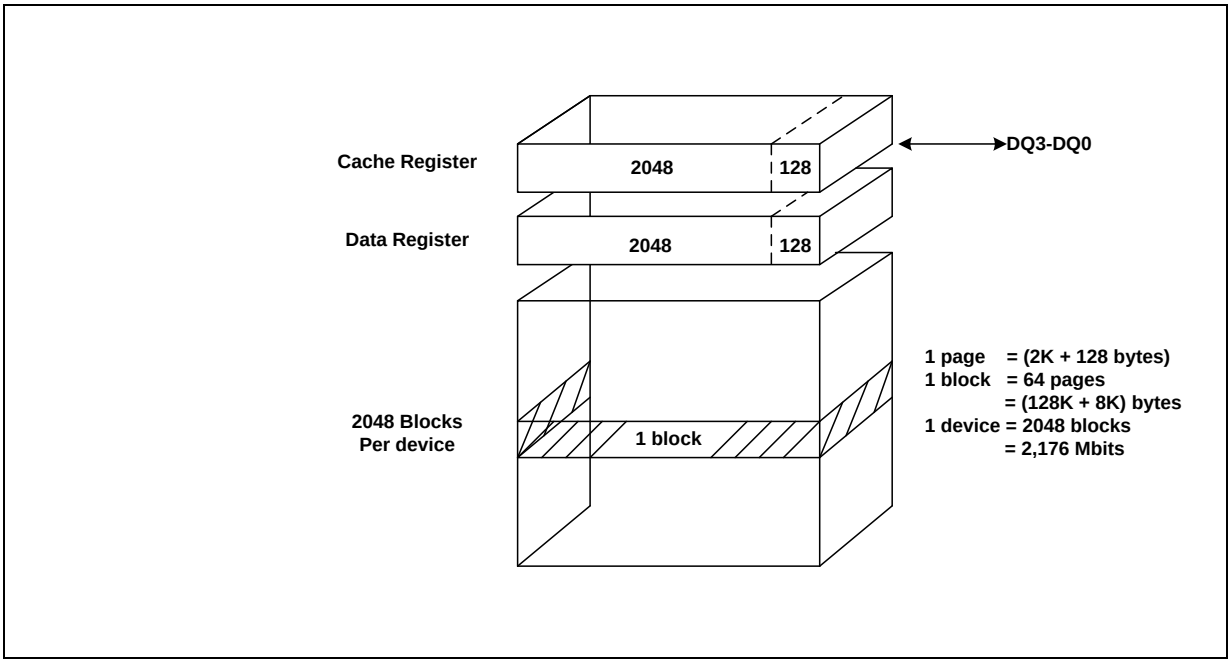
1. **CA**: Column Address. The 12-bit column address is capable of addressing from 0 to 4095 bytes; however,only bytes 0 through 2175 are valid. Bytes 2176 through 4095 of each page are “out of bounds, ” do not exists in the device, and cannot be addressed.
2. **RA**: Row Address. RA<5:0> selects a page inside a block, and RA<16:6> selects a block.

6. Array Organization

Table 2 Array Organization

Each device has	Each block has	Each page has	Unit
128M + 8M	128K + 8K	2K + 128	bytes
2048 x 64	64	-	Pages
2048	-	-	Blocks

Figure 4 Array Organization



7. Device Operations

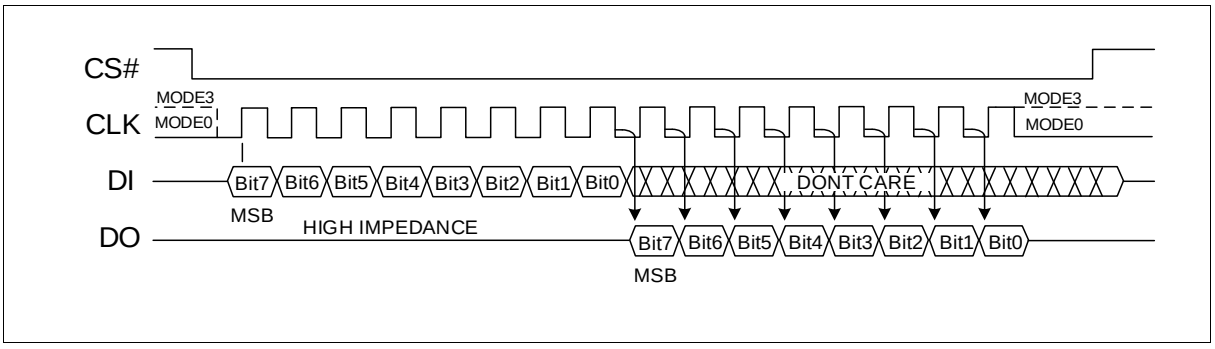
7.1. Single Data Rate (SDR)

7.1.1. Standard SPI

The FM25S02BI3 is accessed through an SPI compatible bus consisting of four signals: Serial Clock (CLK), Chip Select (CS#), Serial Data Input (DI) and Serial Data Output (DO). Standard SPI instructions use the DI input pin to serially write instructions, addresses or data to the device on the rising edge of CLK. The DO output pin is used to read data or status from the device on the falling edge of CLK.

SPI bus operation Mode 0 (0,0) and 3 (1,1) are supported. The primary difference between Mode 0 and Mode 3 concerns the normal state of the CLK signal when the SPI bus master is in standby and data is not being transferred to the Serial Flash. For Mode 0, the CLK signal is normally low on the falling and rising edges of CS#. For Mode 3, the CLK signal is normally high on the falling and rising edges of CS#.

Figure 5 SPI SDR Modes Supported



7.1.2. Dual SPI

The FM25S02BI3 supports Dual SPI operation when using the x2 and dual IO instructions. These instructions allow data to be transferred to or from the device at two times the rate of ordinary Serial Flash devices. When using Dual SPI instructions, the DI and DO pins become bidirectional I/O pins: DQ_0 and DQ_1.

7.1.3. Quad SPI

The FM25S02BI3 supports Quad SPI operation when using the x4 and Quad IO instructions. These instructions allow data to be transferred to or from the device four times the rate of ordinary Serial Flash. When using Quad SPI instructions the DI and DO pins become bidirectional DQ_0 and DQ_1 and the WP # and HOLD# pins become DQ_2 and DQ_3 respectively. Quad SPI instructions require the Quad Enable bit (QE) to be set.

7.2. CS#

The SPI Chip Select (CS#) pin enables and disables device operation. When CS# is high, the device is deselected and the Serial Data Output (DO, or DQ_0, DQ_1, DQ_2, DQ_3) pins are at high impedance. When deselected, the devices power consumption will be at standby levels unless an internal page read, erase, program, read, reset is in progress. When CS# is brought low, the device will be selected, power consumption will increase to active levels and instructions can be written to and data read from the device. After power-up, CS# must transition from high to low before a new instruction will be accepted.

7.3. CLK

This input signal provides the synchronization reference for the SPI interface. Instructions, addresses, or data input are latched on the rising edge of the CLK signal. Data output changes after the falling edge of CLK.

7.4. Serial Input (DI) / DQ0

This input signal is used to transfer data serially into the device. It receives instructions, addresses, and data to be programmed. Values are latched on the rising edge of serial CLK clock signal.

DI becomes DQ0 – an input and output during Dual and Quad commands for receiving instructions, addresses, and data to be programmed (values latched on rising edge of serial CLK clock signal) as well as shifting out data (on the falling edge of CLK).

7.5. Serial Output (DO) / DQ1

This output signal is used to transfer data serially out of the device. Data is shifted out on the falling edge of the serial CLK clock signal.

DO becomes DQ1 – an input and output during Dual and Quad commands for receiving addresses, and data to be programmed (values latched on rising edge of serial CLK clock signal) as well as shifting out data (on the falling edge of CLK).

7.6. Write Protect (WP#) / DQ2

When WP# is driven Low (V_{IL}), during a SET FEATURE command and while the BRWD bit of the Status Register is set to a 1, it is not possible to write to the Status Registers. This prevents any alteration of the Block Protect (BP2, BP1,BP0), TB and CMP bits of the Status Register. As a consequence, all the data bytes in the memory area that are protected by the Block Protect (BP2, BP1,BP0), TB and CMP bits, are also hardware protected against data modification if WP# is Low during a SET FEATURE command.

The WP# function is replaced by DQ2 for input and output during Quad mode for receiving addresses, and data to be programmed (values are latched on rising edge of the CLK signal) as well as shifting out data (on the falling edge of CLK).

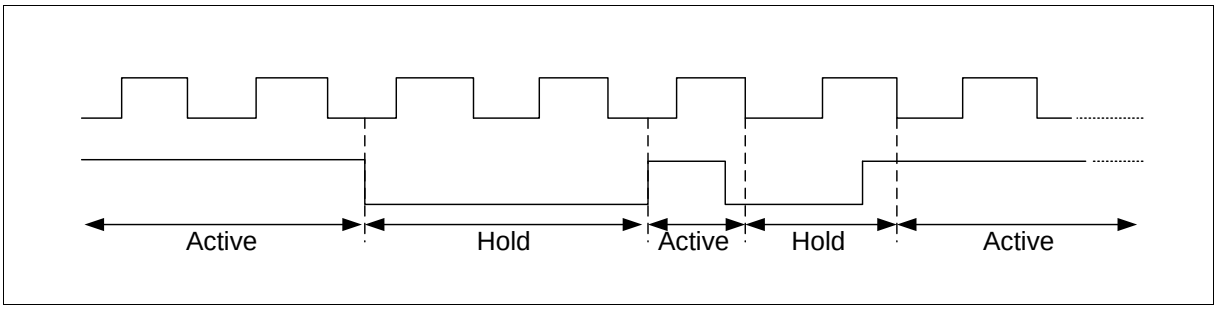
7.7. Hold (HOLD#) / DQ3

For Standard SPI and Dual SPI operations, the HOLD# signal allows the FM25S02BI3 operation to be paused while it is actively selected (when CS# is low). The HOLD# function may be useful in cases where the SPI data and clock signals are shared with other devices. For example, consider if the page buffer was only partially written when a priority interrupt requires use of the SPI bus. In this case the HOLD# function can save the state of the instruction and the data in the buffer so programming can resume where it left off once the bus is available again.

To initiate a HOLD# condition, the device must be selected with CS# low. A HOLD# condition will activate on the falling edge of the HOLD# signal if the CLK signal is already low. If the CLK is not already low the HOLD# condition will activate after the next falling edge of CLK. The HOLD# condition will terminate on the rising edge of the HOLD# signal if the CLK signal is already low. If the CLK is not already low the HOLD# condition will terminate after the next falling edge of CLK. During a HOLD# condition, the Serial Output (DO) is high impedance, and Serial Input (DI) and Serial Clock (CLK) are ignored. The Chip Select (CS#) signal should be kept active (low) for the full duration of the HOLD# operation to avoid resetting the internal logic state of the device.

The HOLD# function is not available when the Quad mode is enabled (QE =1). The Hold function is replaced by DQ3 for input and output during Quad mode for receiving addresses, and data to be programmed (values are latched on rising edge of the CLK signal) as well as shifting out data (on the falling edge of CLK).

Figure 6 Hold Condition Waveform

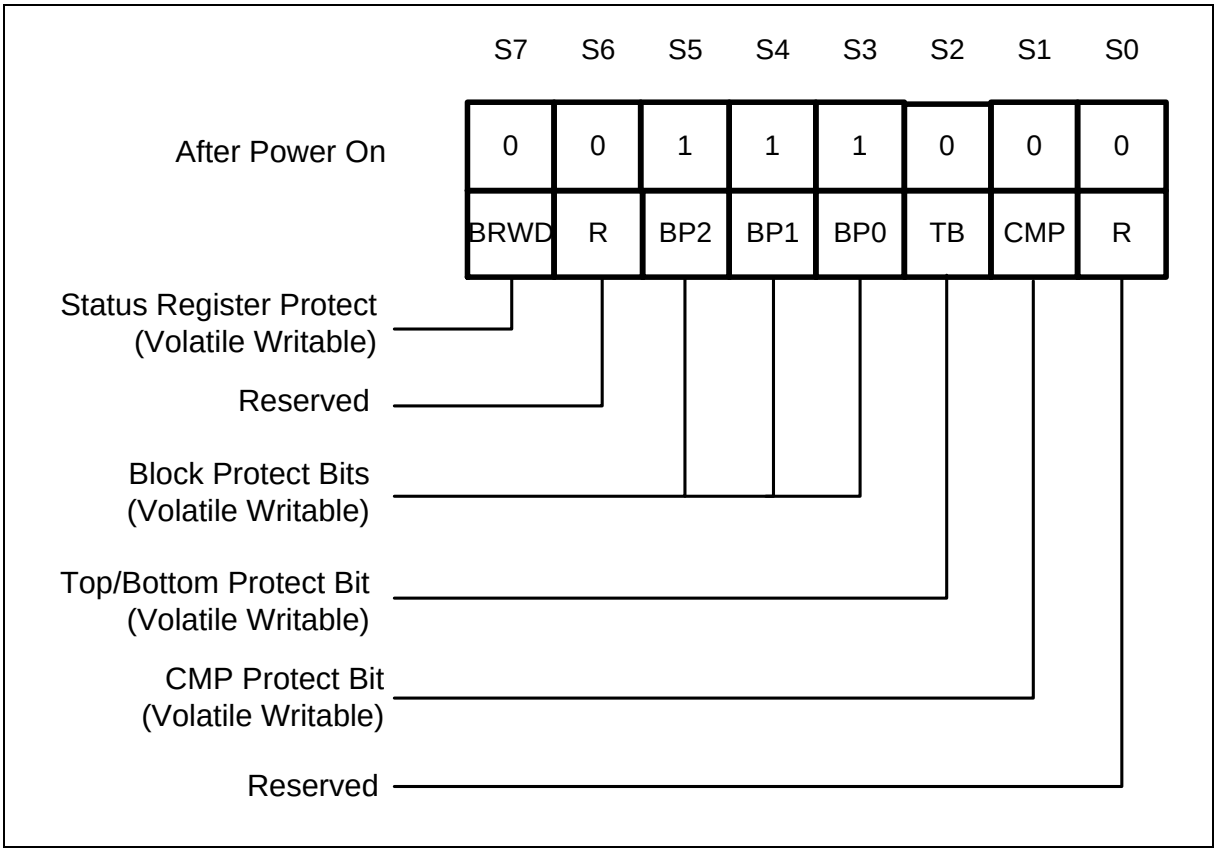


8. Status Register

Four Status Registers are provided for FM25S02BI3:Protection Register (SR-1), Configuration Register (SR-2) and Status Register (SR-3) and Drive Register (SR-4). Each register is accessed by GET FEATURE and SET FEATURE commands combined with 1-Byte Register Address respectively.

8.1. Protection Register/Status Register-1(Volatile Writable)

Figure 7 Protection Register / Status Register-1 (Address A0h)



8.1.1. Block Protection Bits (CMP, BP2, BP1, BP0, TB)

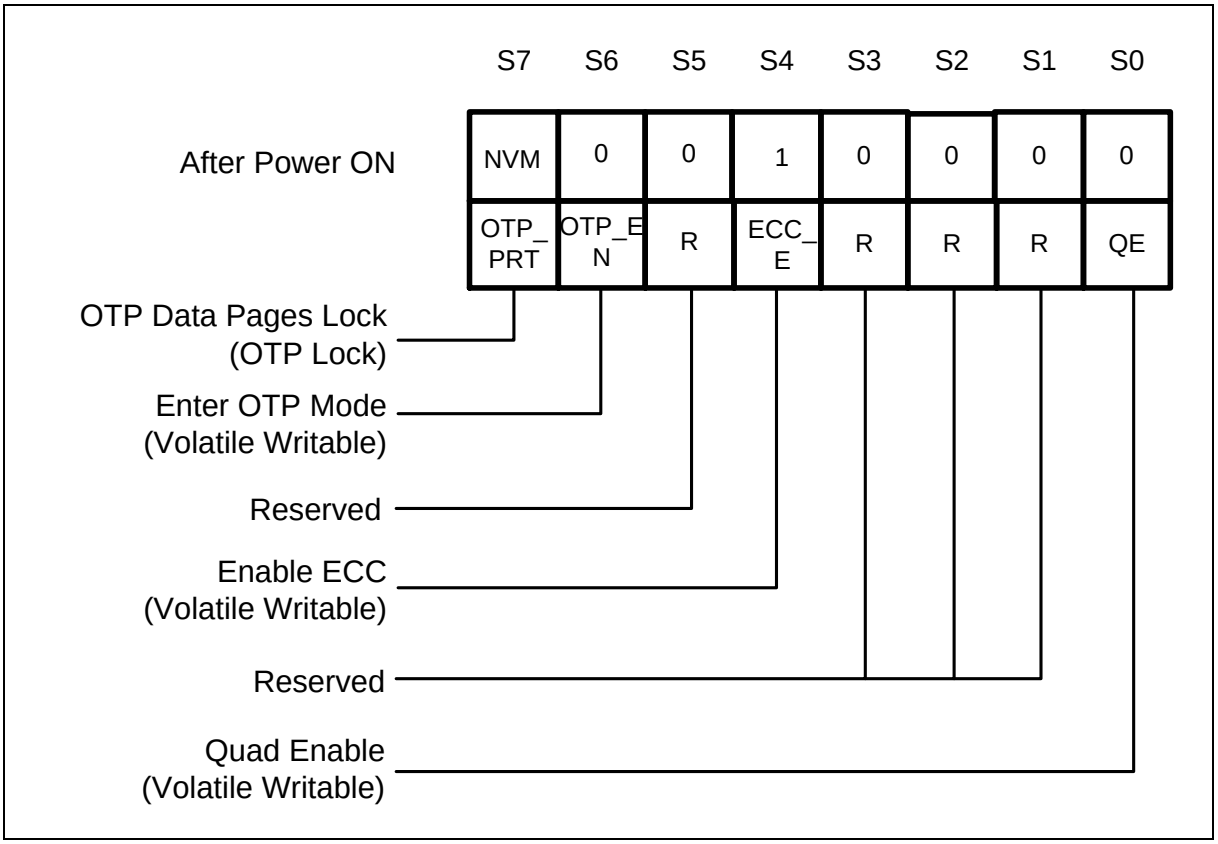
The Block Protect bits (CMP, BP2, BP1, BP0&TB) are volatile read/write bits in the status register-1 that provide Write Protection control and status. Block Protect bits can be set using the Write Status Register Instruction. All, none or a portion of the memory array can be protected from Program and Erase instructions (See Status Register Memory Protection table). The default values for the Block Protection bits(BP2,BP1,BP0) are 1 after power up to protect the entire array.

8.1.2. Block Register Write Protection Bit (BRWD)

The block lock feature provides the ability to protect the entire device, or ranges of blocks, from the PROGRAM and ERASE operations. After power-up, the device is in the “locked” state, i.e., feature bit BP0,BP1 and BP2 are set to 1, TB, CMP and BRWD are set to 0. To unlock all the blocks, or a range of blocks, the Write Status Register command must be issued to alter the state of protection feature bit. When BRWD is set and WP# is LOW, none of the writable protection feature bits can be set.

8.2. Configuration Register/Status Register-2

Figure 8 Configuration Register/ Status Register-2 (Address B0h)



8.2.1. One Time Program Lock Bit(OTP_PRT) — OTP Lockable

In addition to the main memory array, FM25S02BI3 also provides an OTP area for the system to store critical data that cannot be changed once it's locked. The OTP area consists of 25 pages of 2176-Byte each. The default data in the OTP area are FFh. Only Program command can be issued to the OTP area to change the data from "1" to "0" , and data is not reversible ("0" to "1") by the Erase command. Once the correct data is programmed in and verified, the system developer can set OTP_PRT bit to 1, so that the entire OTP area will be locked to prevent further alteration to the data.

8.2.2. Enter OTP Access Mode Bit(OTP_EN) — Volatile Writable

The OTP_EN bit must be set to 1 in order to use the standard Program/Read commands to access the OTP area as well as to read the Unique ID/ Parameter Page information. The default value after power up or a RESET command is 0.

8.2.3. ECC Enable Bit (ECC_E) — Volatile Writable

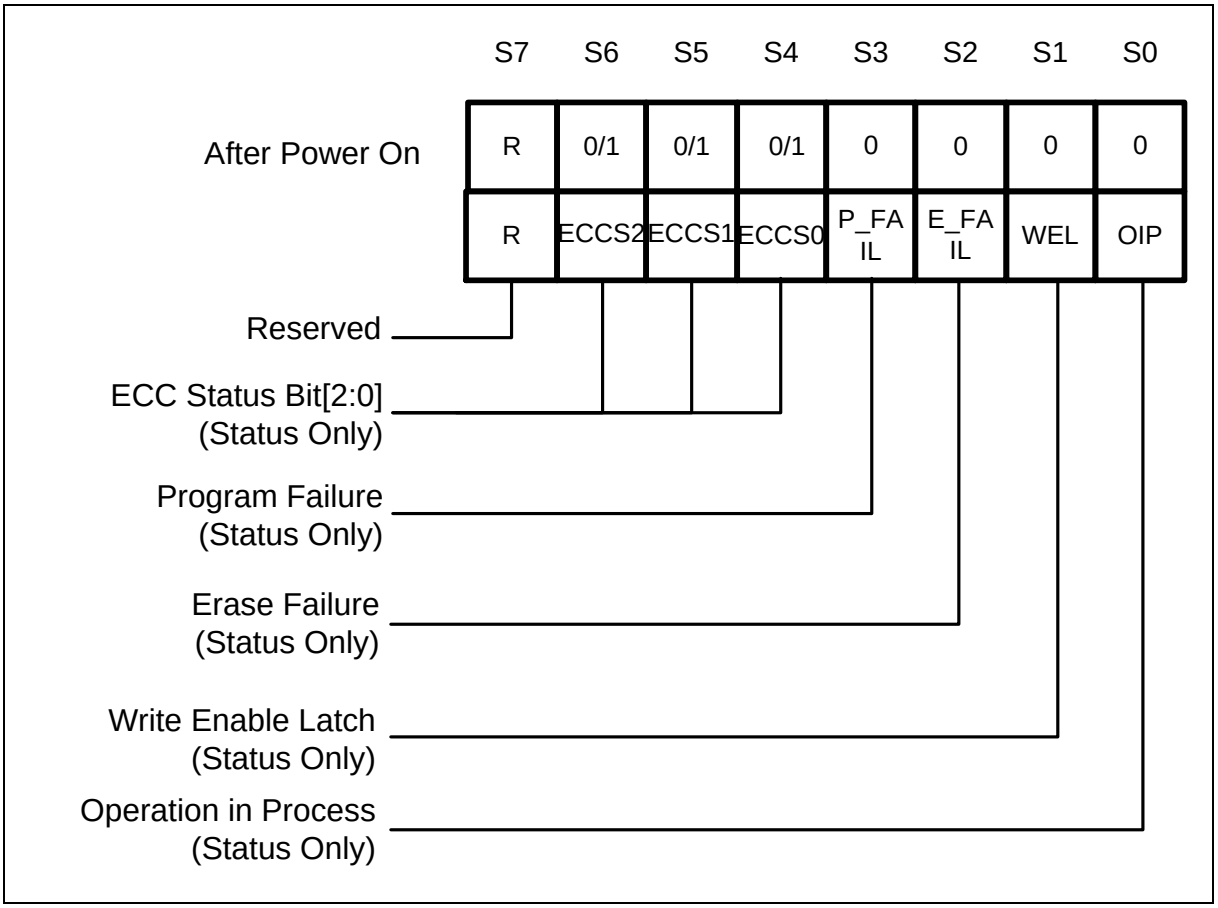
FM25S02BI3 has a built-in ECC algorithm that can be used to preserve the data integrity. Internal ECC calculation is done during page programming, and the result is stored in the extra area for each page. During the data read operation, ECC engine will verify the data values according to the previously stored ECC information and to make necessary corrections if needed. The verification and correction status is indicated by the ECC Status Bits. ECC function is enabled by default when power on (ECC_E=1), and it will not be reset to 0 by the Device Reset command.

8.2.4. QE Bit(QE) — Volatile Writable

The QE bit must be set to 1 before Quad instruction is issued.

8.3. Status Register-3

Figure 9 Status Register-3 (Address C0h)



8.3.1. Cumulative ECC Status(ECCS2,ECCS1,ECCS0) —Status Only

ECC function is used in NAND flash memory to correct limited memory errors during read operations. The ECC Status Bits (ECCS2,ECCS1, ECCS0) should be checked after the completion of a Read operation to verify the data integrity. The ECC Status bits values are don't care if ECC_E=0. These bits will be cleared to 0 after a RESET command.
After power-on, ECC status is set to reflect the contents of block 0, page 0.

Table 3 ECC Status Bits

ECC Status			Description
ECCS1	ECCS1	ECCS0	
0	0	0	No errors
0	0	1	1-bit to 3-bit error detected and corrected
0	1	0	more than 8-bit errors detected and not corrected
0	1	1	4-bit to 6-bit error detected and corrected
1	0	1	7-bit to 8-bit error detected and corrected

8.3.2. Program/Erase Failure(P_FAIL, E_FAIL) —Status Only

The Program/Erase Failure Bits are used to indicate whether the internally-controlled Program/Erase operation was executed successfully or not. These bits will also be set respectively when the Program or Erase command is issued to a locked or protected memory or OTP area. Both bits will be cleared at the beginning of the Program Execute or Block Erase instructions as well as the device RESET instruction.

8.3.3. Write Enable Latch(WEL) —Status Only

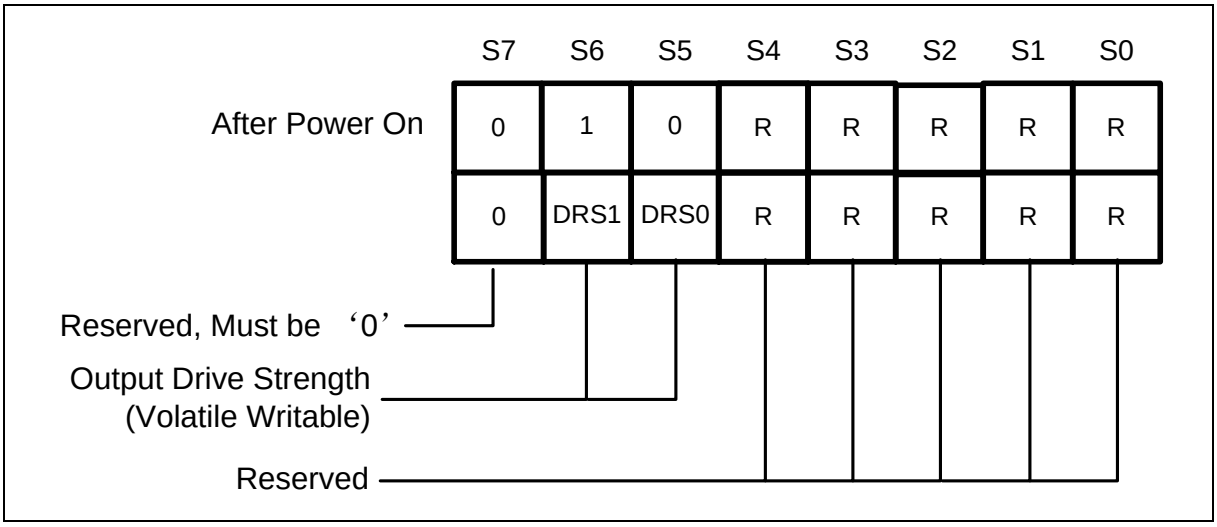
Write Enable Latch (WEL) is a read only bit in the status register that is set to 1 after executing a Write Enable Instruction. The WEL status bit is cleared to 0 when the device is write disabled. A write disable state occurs upon power-up or after any of the following instructions: Write Disable, Program Execute, Block Erase, Program Execute for OTP pages, and OTP locking.

8.3.4. Operation In Progress(OIP) —Status Only

OIP is a read only bit in the status register that is set to a 1 state when the device is powering up or executing a Page Data Read, Program Execute, Block Erase, Program Execute for OTP area, OTP Locking and RESET instruction. During this time the device will ignore further instructions except for the GET FEATURE, RESET and Read ID instructions. When the program, erase or page read instruction has completed, the OIP bit will be cleared to a 0 state indicating the device is ready for further instructions.

8.4. Configure Register-4

Figure 10 Status Register-4 (Address D0h)



8.4.1. Drive Strength (DRS1, DRS0) — Volatile Writable

Output Drive Strength bit can be used to adjust output PAD strength.
For FM25S02BI3, default Drive Strength bit (DRS1, DRS0) is (1,0), which means default Drive Strength is 50%.

Table 4 Drive Strength Bits

DRS1	DRS0	Driver Strength
0	0	100%
0	1	75%
1	0	50%
1	1	25%

9. Command Definition

9.1. Command Set Tables

Table 5 Standard SPI Command Set

INSTRUCTION NAME	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE N
WRITE ENABLE	**06h**					
WRITE DISABLE	**04h**					
GET FEATURE	**0Fh**	A7-A0	(D7-D0)			
SET FEATURE	**1Fh**	A7-A0	D7-D0			
PAGE READ （to cache）	**13h**	A23-A16	A15-A8	A7-A0		
READ FROM CACHE	**03h/0Bh**	A15-A8(2)	A7-A0	dummy	(D7-D0)	Byte N
READ ID	**9Fh**	dummy	(MID) (8)	(DID) (8)		
PROGRAM LOAD	**02h**	A15-A8(6)	A7-A0	D7-D0	Next byte	Byte N
PROGRAM LOAD RANDOM DATA	**84h**	A15-A8(6)	A7-A0	D7-D0	Next byte	Byte N
PROGRAM EXECUTE	**10h**	A23-A16	A15-A8	A7-A0		
BLOCK ERASE	**D8h**	A23-A16	A15-A8	A7-A0		
RESET	**FFh**					

Table 6 Dual SPI Command Set

INSTRUCTION NAME	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE N
READ FROM CACHE x 2	**3Bh**	A15-A8(2)	A7-A0	dummy	(D7-D0)x2	Byte N

Table 7 Quad SPI Command Set

INSTRUCTION NAME	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE N
READ FROM CACHE x4	**6Bh**	A15-A8(2)	A7-A0	dummy	(D7-D0)x4	Byte N
PROGRAM LOAD x4	**32h**	A15-A8(6)	A7-A0	(D7-D0)x4	Next byte	Byte N
PROGRAM LOAD RANDOM DATA x4	**34h**	A15-A8(6)	A7-A0	(D7-D0)x4	Next byte	Byte N

Notes:

1. Data bytes are shifted with Most Significant Bit first. Byte fields with data in parenthesis “( )” indicate data output from the device on either 1, 2 or 4 DQ pins.
2. The x8 clock = 4’b0, A11-A8
3. The x8 clock = 4’b0, A11-A0
4. The x8 clock = dummy<7:0>,D7-D0
5. The x8 clock = 4’b0,A11-A0,dummy<15:0>
6. The x8 clock = dummy<3:0>,A11-A8
7. MID is Manufacture ID , DID is Device ID(D6h for current device)

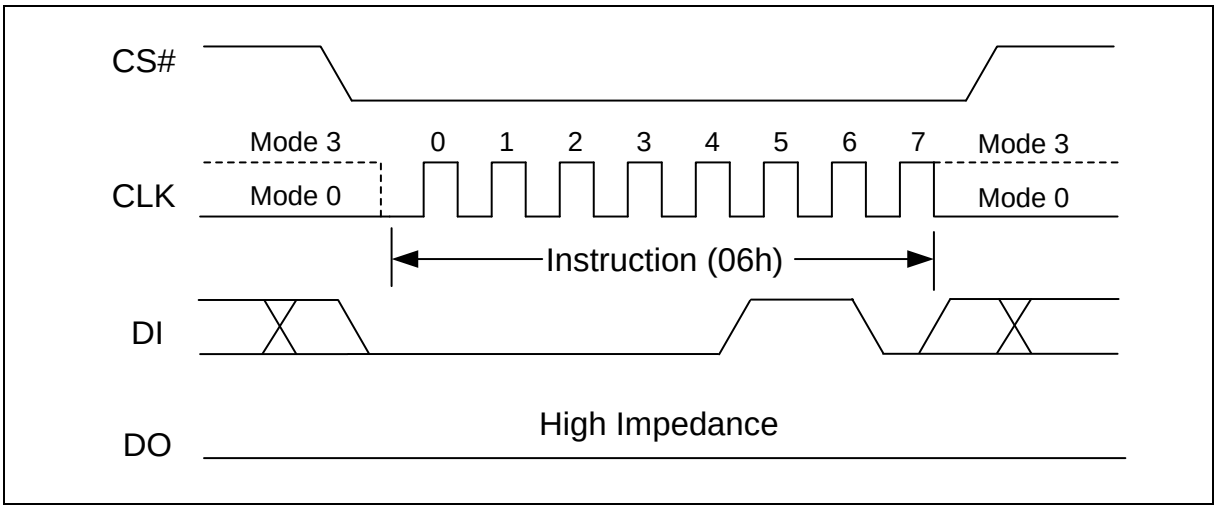
9.2. WRITE operation

9.2.1. WRITE ENABLE (WREN) (06h)

The WRITE ENABLE (WREN) command sets the WEL bit in the status register to 1. The WEL bit must be set prior to following operations that changes the contents of the memory array:

- PAGE PROGRAM
- OTP PROGRAM
- OTP LOCK
- BLOCK ERASE

Figure 11 WRITE ENABLE (06h) Timing

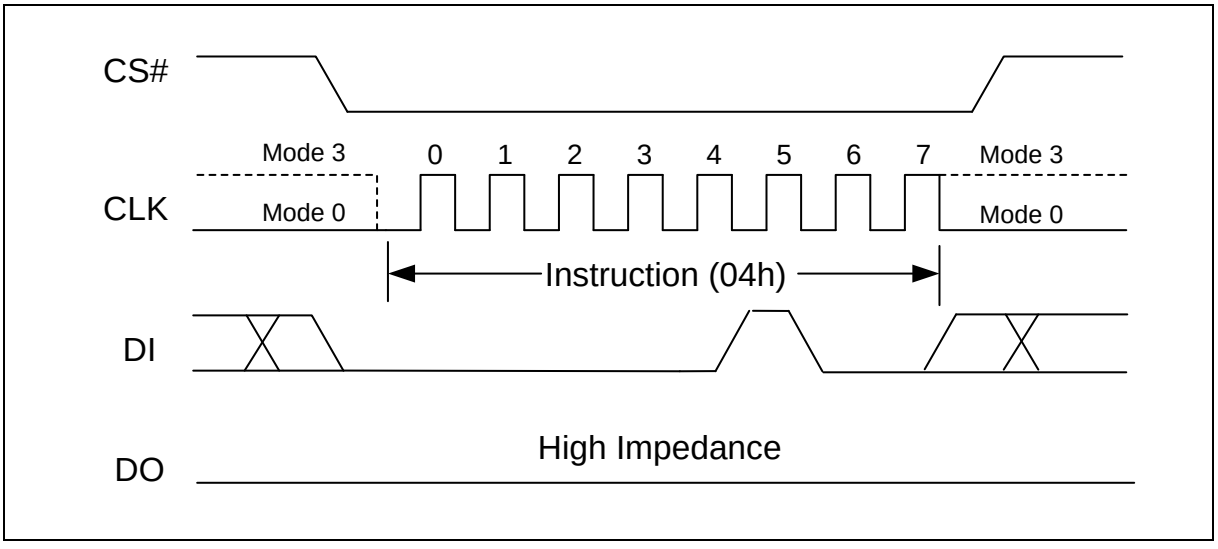


9.2.2. WRITE DISABLE (WRDI) (04h)

The WRITE DISABLE (WRDI) command resets the WEL bit in the status register to 0. The WEL bit is automatically reset after Power-up and upon completion of the following operations:

- PAGE PROGRAM
- OTP PROGRAM
- OTP LOCK
- BLOCK ERASE

Figure 12 WRITE DISABLE (04h) Timing



9.3. Feature Operation

9.3.1. GET FEATURE (0Fh) and SET FEATURE (1Fh)

The GET FEATURE (0Fh) and SET FEATURE (1Fh) commands are used to alter the device behavior from the default power-on behavior. These commands use a 1-byte feature address to determine which feature is to be read or modified. Features such as OTP and block protection can be enabled or disabled by setting specific bits in feature address A0h and B0h (shown the following table). The status register is mostly read, except WEL, which is writable bit with the WREN (06h) command.

When a feature is set, it remains active until the device is power cycled or the feature is written to. Unless otherwise specified in the Status Register section, once the device is set, it remains set, even if a RESET (FFh) command is issued.

Table 8 Features Settings

Register	Address	Data Bits							
		7	6	5	4	3	2	1	0
SR-1	**A0h**	BRWD	Reserved	BP2	BP1	BP0	TB	CMP	Reserved
SR-2	**B0h**	OTP_PRT	OTP_EN	Reserved	ECC_E	Reserved	Reserved	Reserved	QE
SR-3	**C0h**	Reserved	ECCS2	ECCS1	ECCS0	P_FAIL	E_FAIL	WEL	OIP
SR-4	**D0h**	DS	DRS1	DRS0	Reserved	Reserved	Reserved	Reserved	Reserved

Figure 13 GET FEATURE (0Fh) Timing

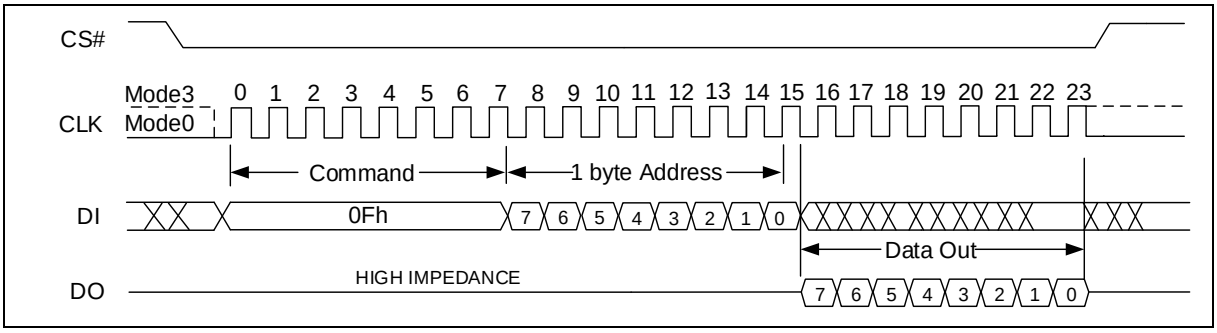
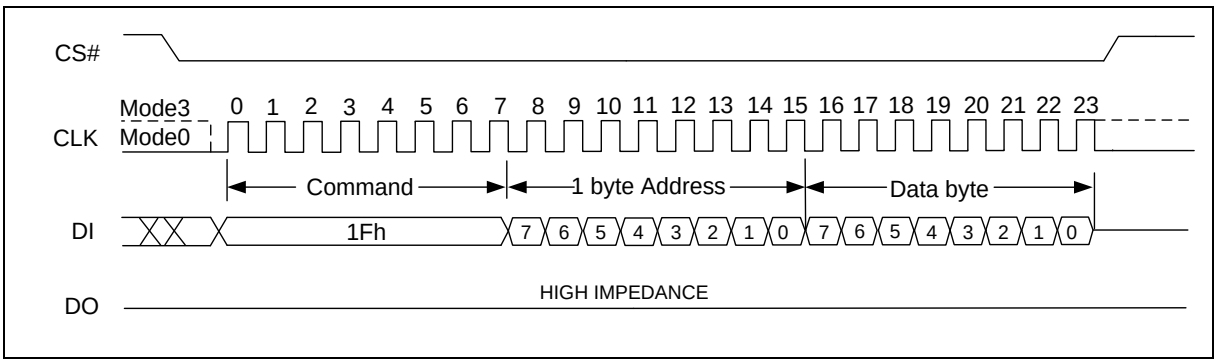


Figure 14 SET FEATURE (1Fh) Timing



9.4. READ Operation

9.4.1. PAGE READ

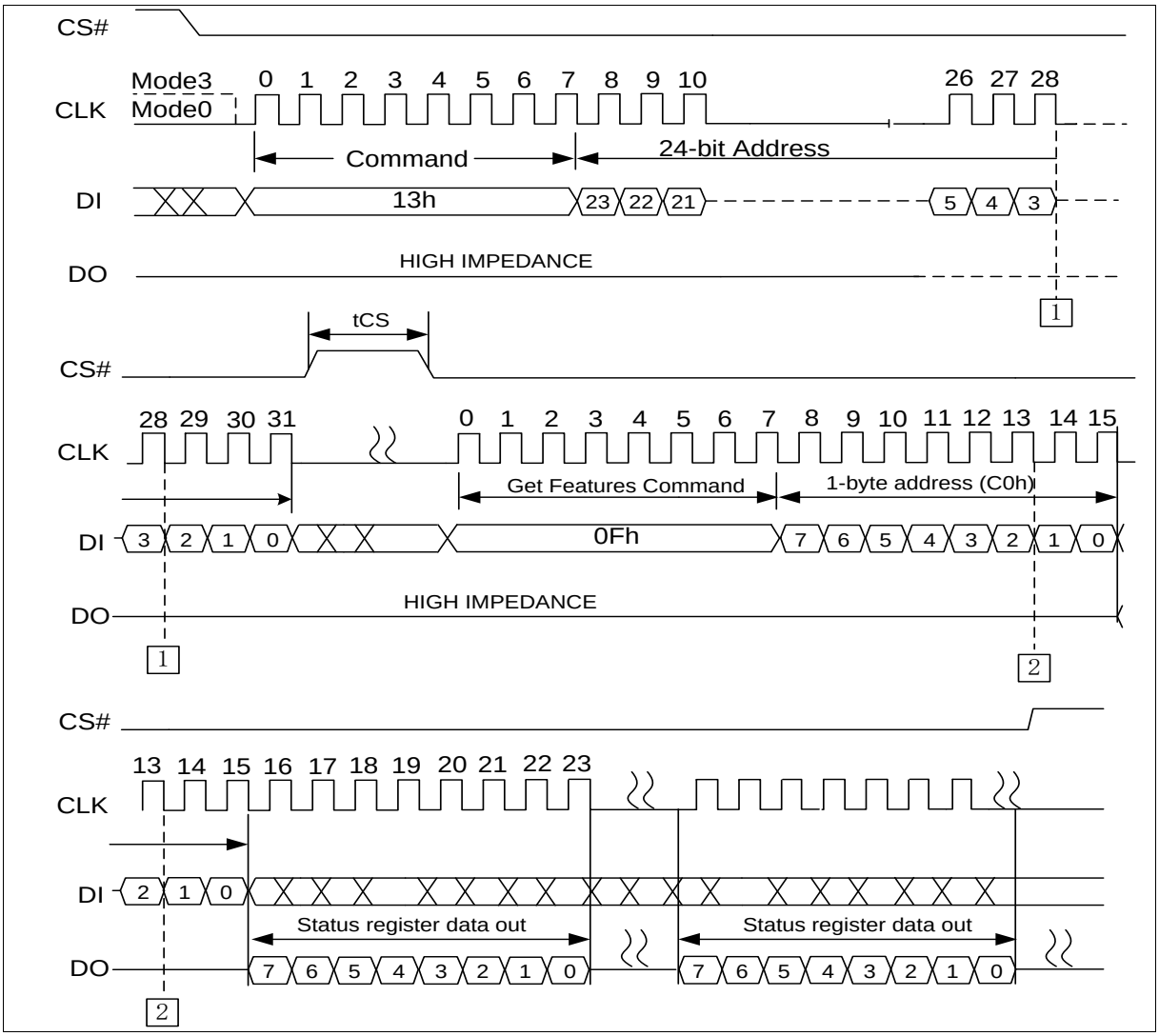
The PAGE READ (13h) command transfers the data from the NAND Flash array to the cache register. The command sequence is follows:

- 13h (PAGE READ TO CACHE)
- 0Fh (GET FEATURE command to read the status)
- READ FROM CACHE Operation
  - 0Bh or 03h (READ FROM CACHE)
  - 3Bh (READ FROM CACHE x2)
  - 6Bh (READ FROM CACHE x4)

The PAGE READ command requires a 24-bit address consisting of 7 dummy bits followed by a 17-bit block/page address. After the block/page addresses are registered, the device starts the transfer from the main array to the cache register, and is busy for t_{RD} time. During this time, the GET FEATURE (0Fh) command can be issued to monitor the status of the operation (refer to the Status Register section). Following a status of successful completion, the READ FROM CACHE (03h/0Bh/3Bh/6Bh) command must be issued in order to read the data out of the cache.

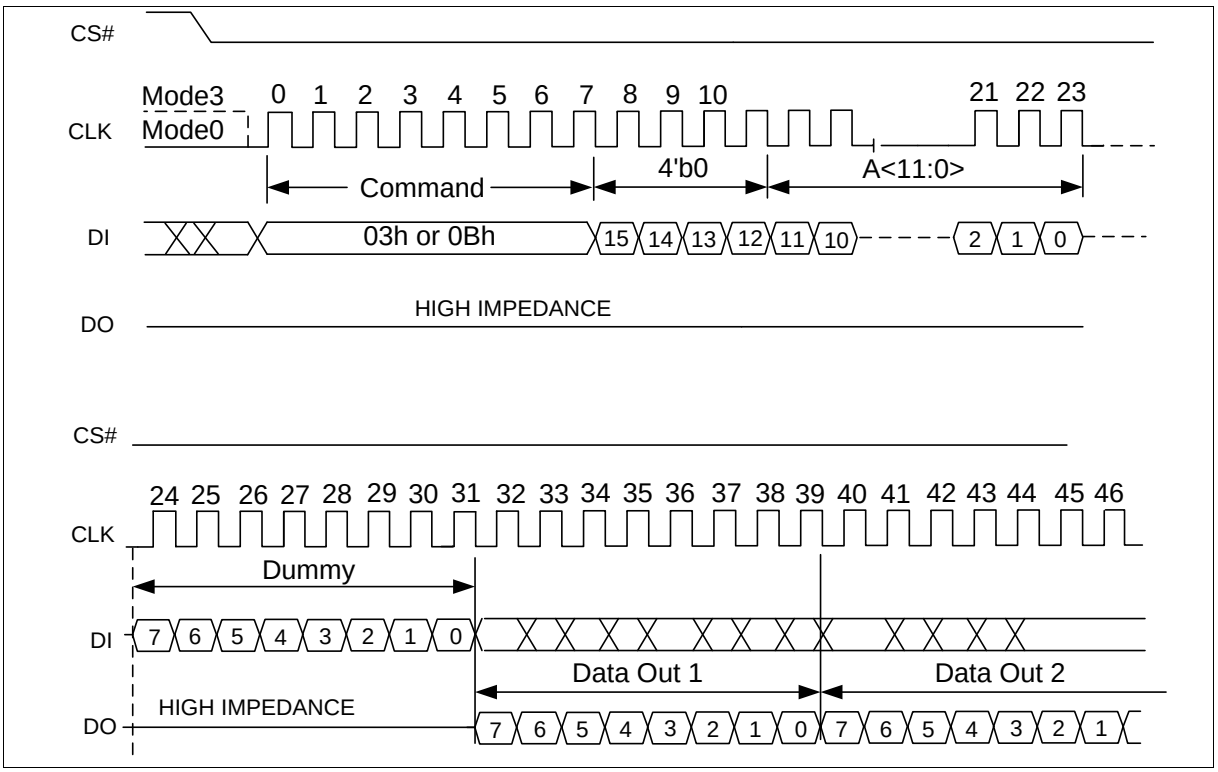
9.4.2. PAGE READ TO CACHE (13h)

Figure 15 Page Read READ CACHE (13h) Timing



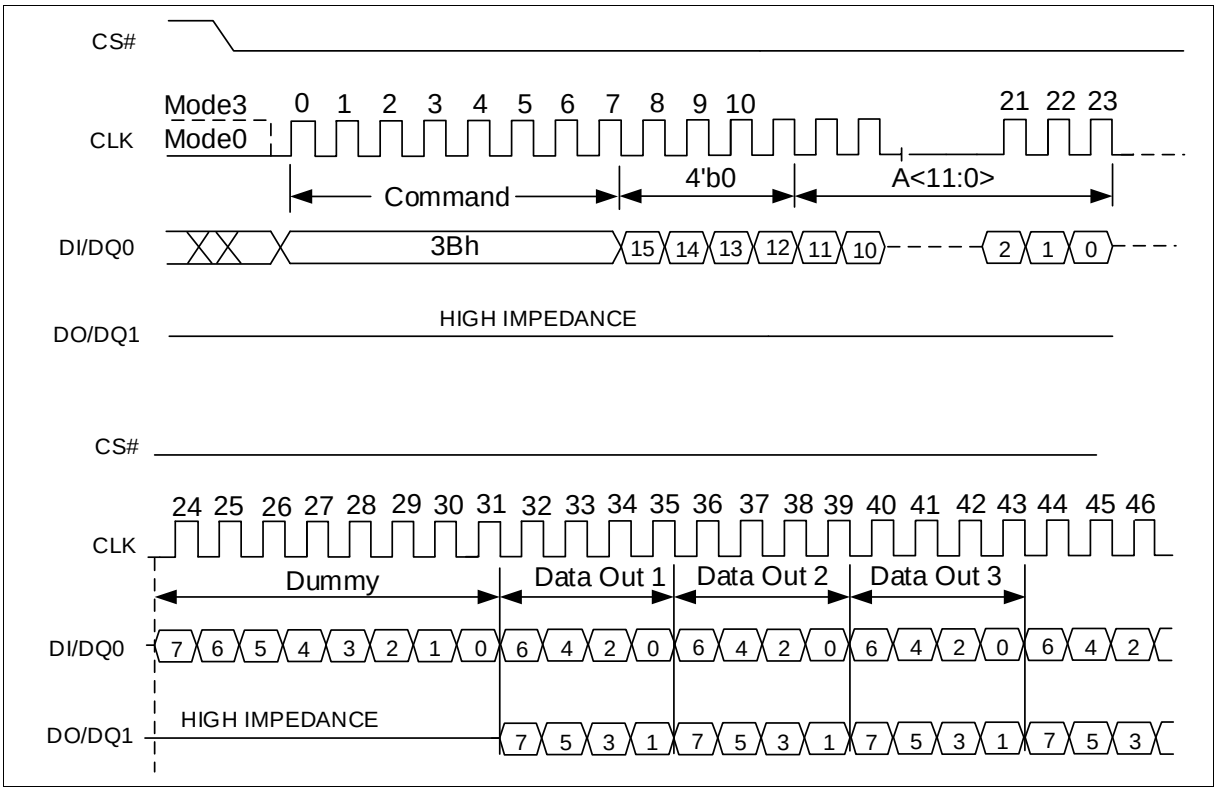
9.4.3. READ FROM CACHE (03h/0Bh)

Figure 16 READ FROM CACHE (03h / 0Bh) Timing



9.4.4. READ FROM CACHE x2 (3Bh)

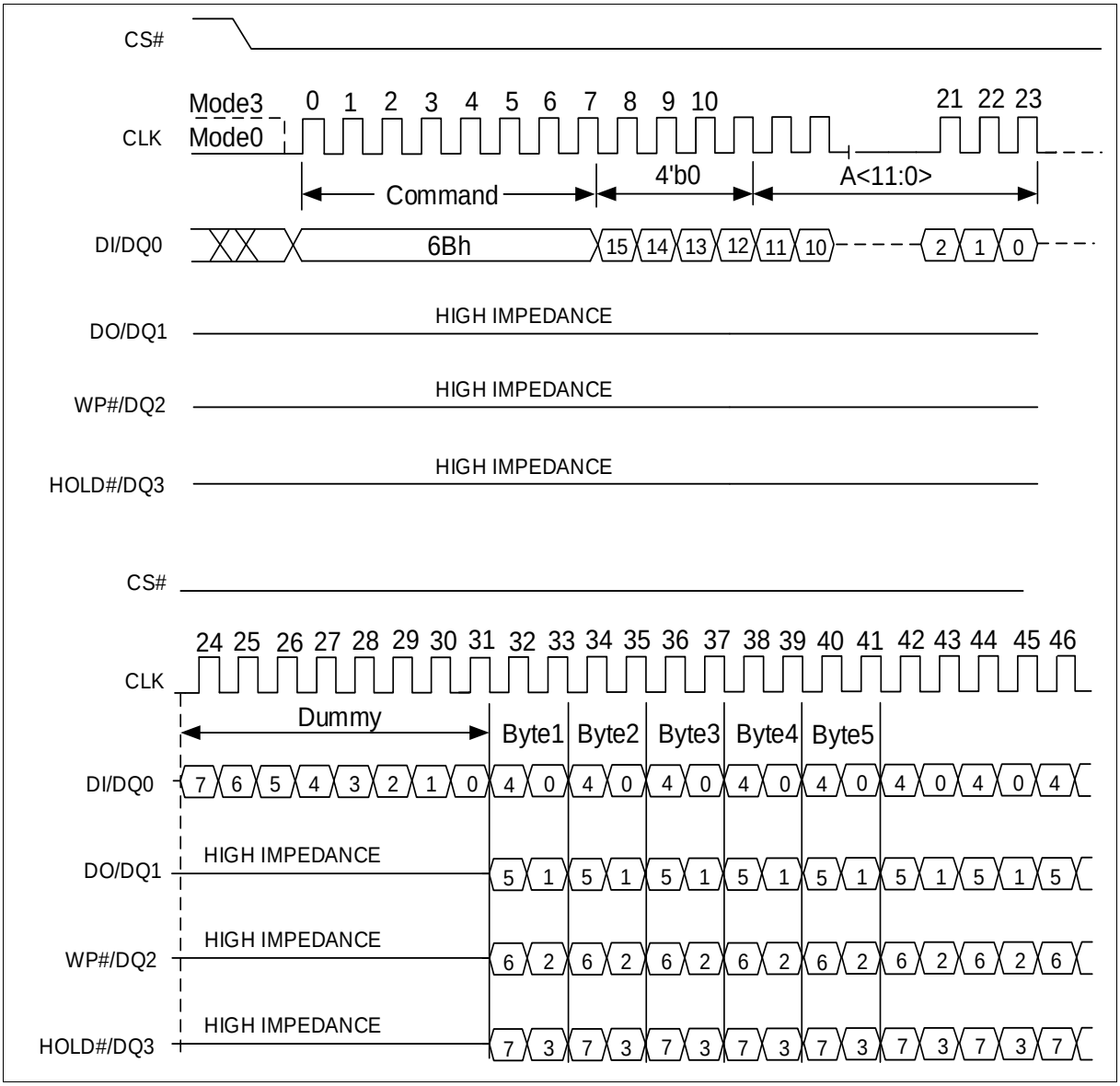
Figure 17 READ FROM CACHE x2 (3Bh) Timing



9.4.5. READ FROM CACHE x4 (6Bh)

The Quad Enable bit (QE) of SR-2 feature register must be set to enable the READ FROM CACHE X4 command.

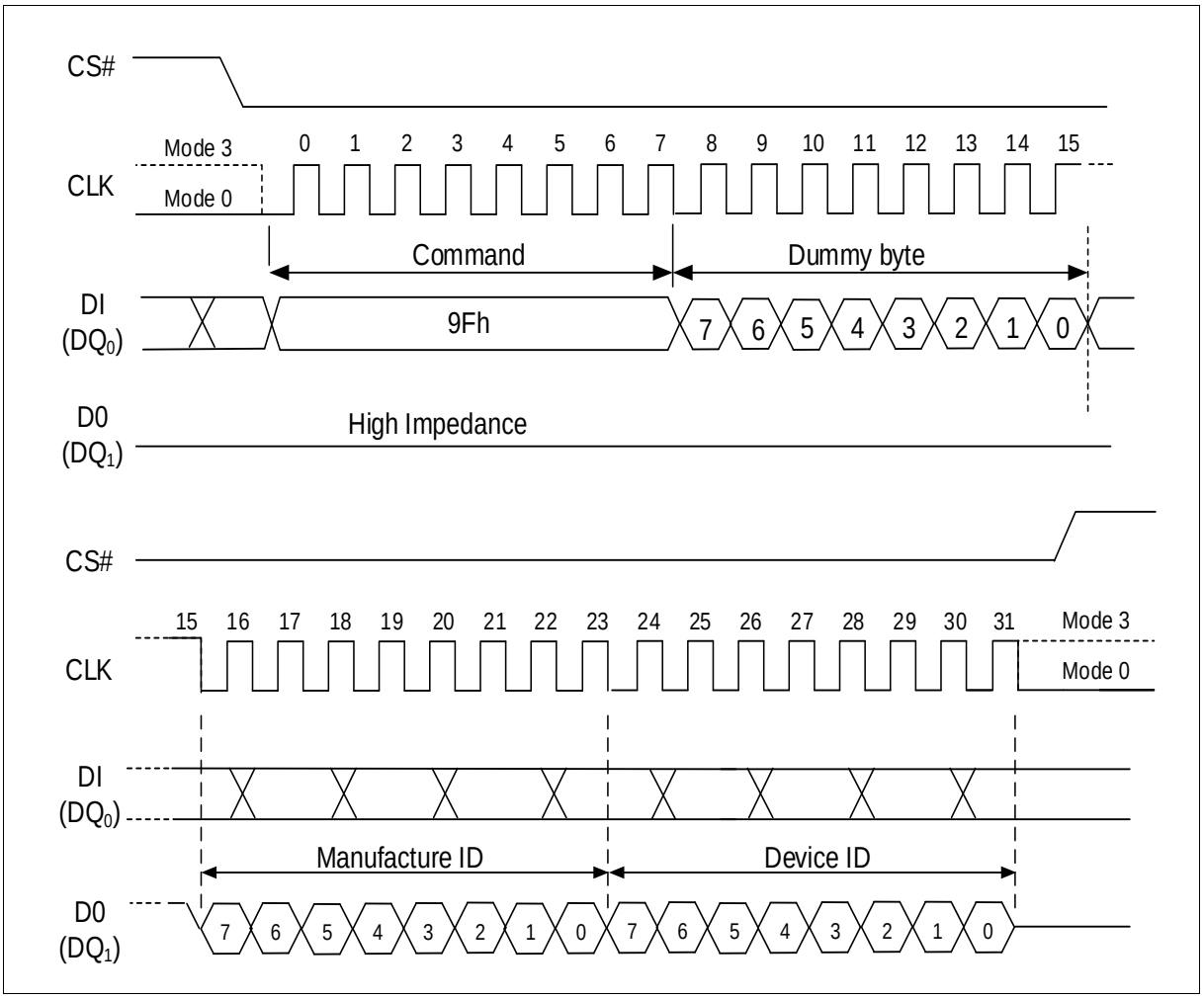
Figure 18 READ FROM CACHE x4 (6Bh) Timing



9.4.6. READ ID (9Fh)

The READ ID command is used to read the 2 bytes of identifier code programmed into the NAND Flash device. The READ ID command reads a 2-byte table that includes the Manufacturer ID and the device configuration.

Figure 19 READ ID (9Fh) Timing



9.5. PROGRAM Operation

The PAGE PROGRAM operation sequence programs 1 byte to 2176 bytes of data within a page. The page program sequence is as follows:

- 02H (PROGRAM LOAD)/32H (PROGRAM LOAD x4)
- 06H (WRITE ENABLE)
- 10H (PROGRAM EXECUTE)
- 0FH (GET FEATURE command to read the status)

The 1st step is to issue a PROGRAM LOAD (02H/32H) command. PROGRAM LOAD consists of an 8-bit Op code, followed by 4 dummy bits and a 12-bit column address, then the data bytes to be programmed. The data bytes are loaded into a cache register which is 2176 bytes long. If more than 2176 bytes are loaded, then those additional bytes are ignored by the cache register. The command sequence ends when CS# goes from LOW to HIGH. Figure 20 shows the PROGRAM LOAD operation.

The 2nd step, prior to performing the PROGRAM EXECUTE operation, is to issue a WRITE ENABLE (06H) command. As with any command that changes the memory contents, the WRITE ENABLE must be executed in order to set the WEL bit. If this command is not issued, then the rest of the program sequence is ignored.

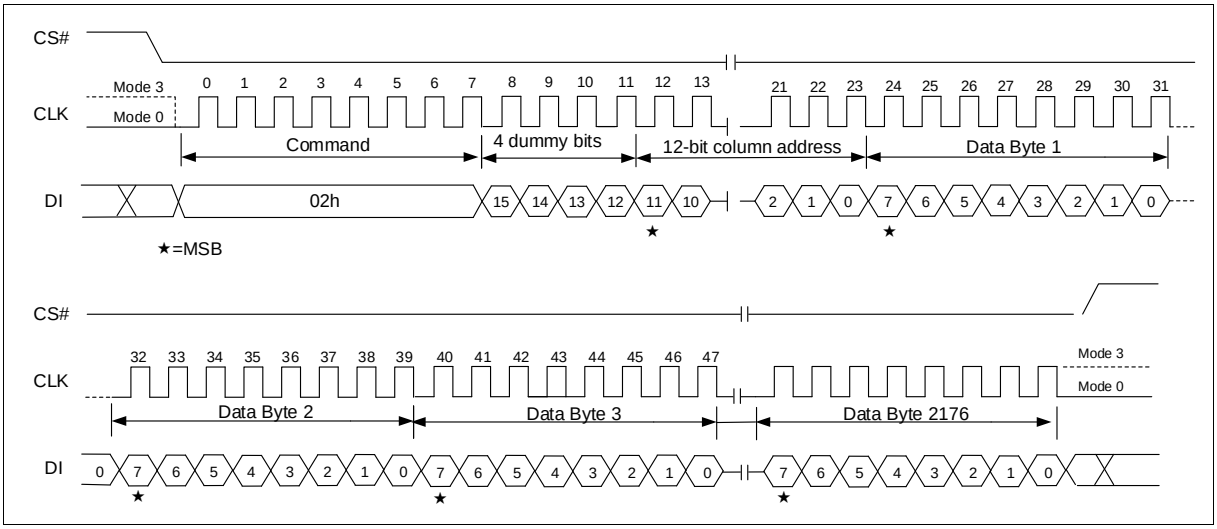
The 3rd step is to issue a PROGRAM EXECUTE (10h) command to initiate the transfer of data from the cache register to the main array. PROGRAM EXECUTE consists of an 8-bit Op code, followed by a 24-bit address (7 dummy bits and a 17-bit page/block address). After the page/block address is registered, the memory device starts the transfer from the cache register to the main array, and is busy for t_{PROG} time. This operation is shown in Figure 22.

During this busy time, the status register can be polled to monitor the status of the operation (refer to the Status Register section). When the operation completes successfully, the next series of data can be loaded with the PROGRAM LOAD command.

Note: The number of consecutive partial page programming operations (NOP) within the same page must not exceed 4. In addition, pages must be sequentially programmed within a block.

9.5.1. PROGRAM LOAD (02h)

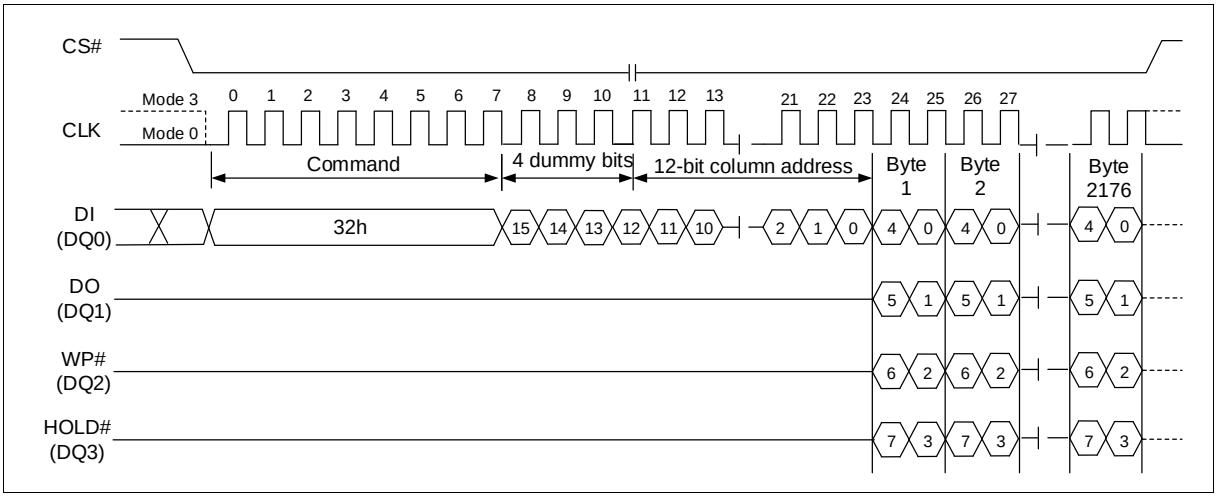
Figure 20 PROGRAM LOAD (02h) Timing



9.5.2. PROGRAM LOAD x4 (32h)

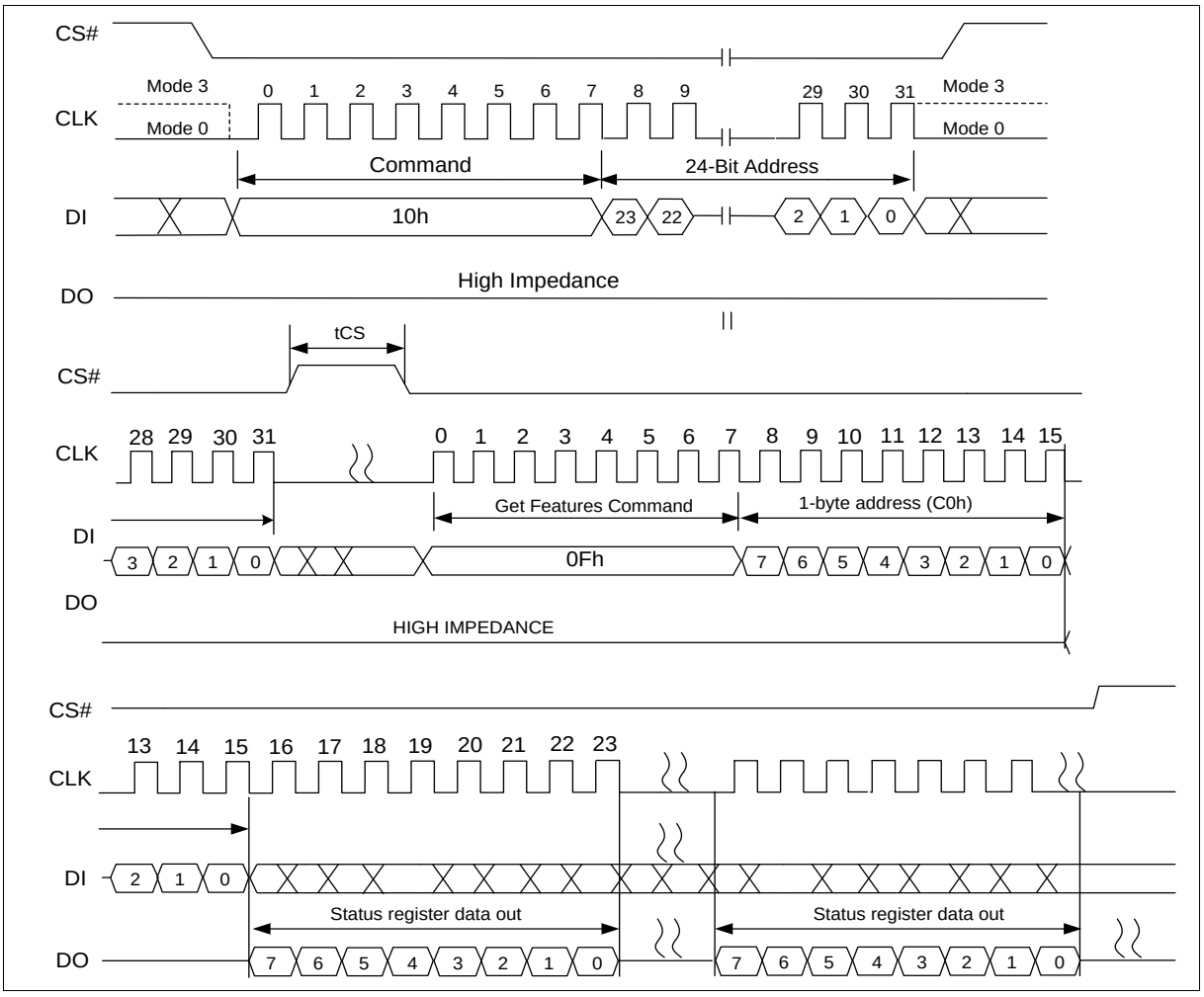
The PROGRAM LOAD x4 command (32H) is similar to the PROGRAM LOAD command (02H) but with the capability to input the data bytes by four pins: DQ0, DQ1, DQ2, and DQ3. The command sequence is shown below.

Figure 21 PROGRAM LOAD x4 (32h) Timing



9.5.3. PROGRAM EXECUTE (PE) (10h)

Figure 22 PROGRAM EXECUTE (10h) Timing



9.5.4. Random Data Program

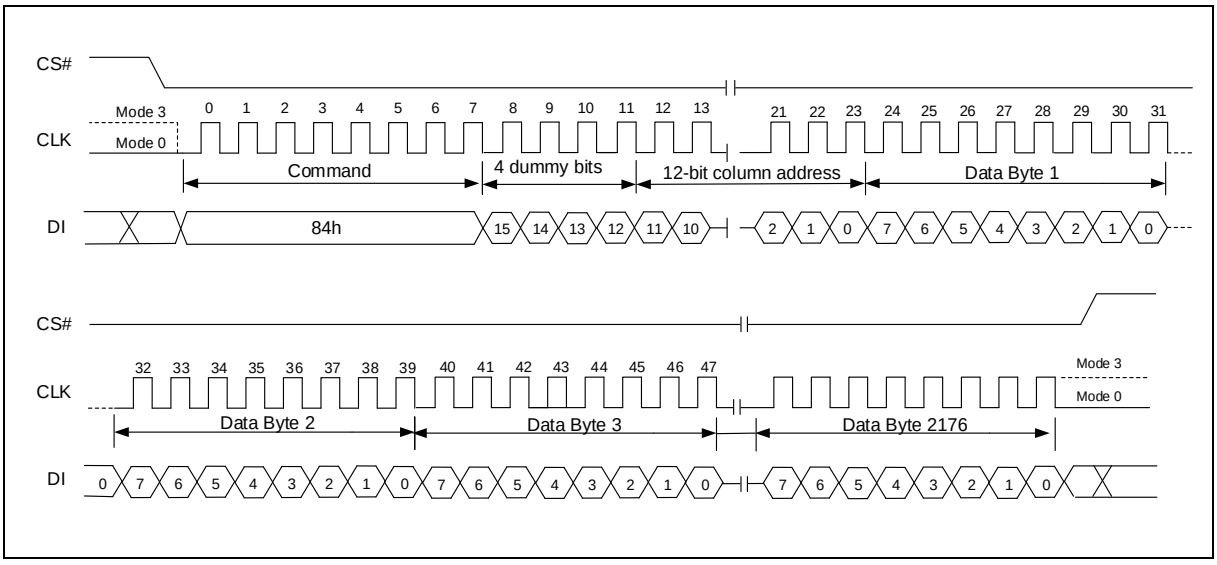
The command sequence is as follows:

- 84h (PROGRAM LOAD RANDOM DATA x1) / 34h (x4)
- 06H (WRITE ENABLE)
- 10H (PROGRAM EXECUTE)
- 0FH (GET FEATURE command to read the status)

The random data program operation sequence programs or replaces data in a page with existing data. PROGRAM LOAD RANDOM DATA command requires 16-bit address with 4 dummy bits and a 12-bit column address. New data is loaded in the column address provided. If the random data is not sequential, then another PROGRAM LOAD RANDOM DATA command must be issued with a new column address. After the data is loaded, PROGRAM EXECUTE command can be issued to start the programming operation.

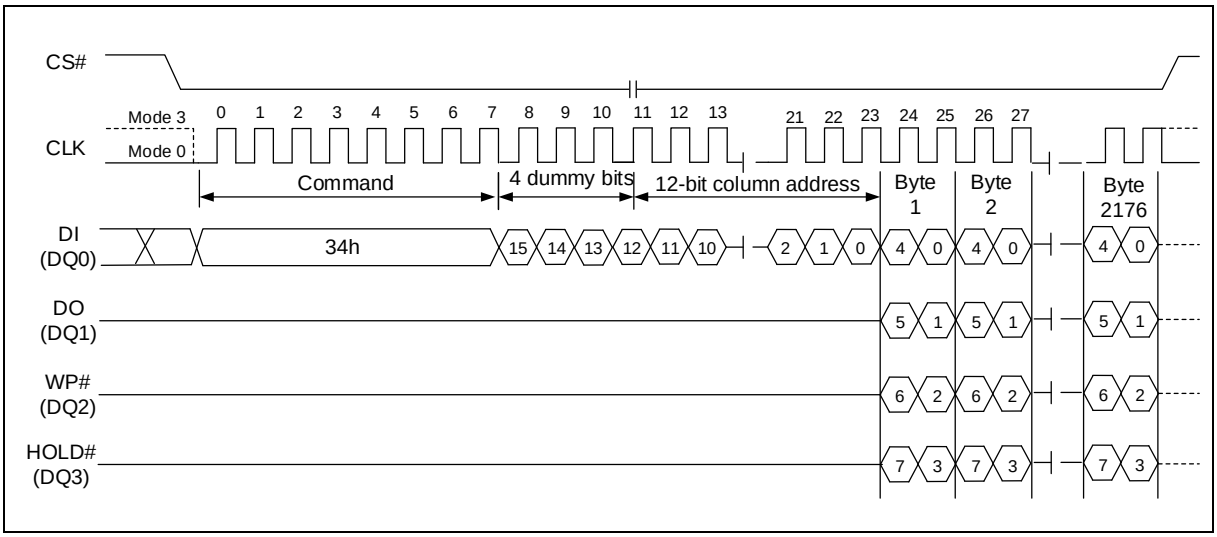
9.5.5. PROGRAM LOAD RANDOM DATA (84h)

Figure 23 PROGRAM LOAD RANDOM DATA (84h) Timing



9.5.6. PROGRAM LOAD RANDOM DATA x4 (34h)

Figure 24 PROGRAM LOAD RANDOM DATA x4 (34h) Timing



9.5.7. INTERNAL DATE MOVE

The INTERNAL DATA MOVE command sequence programs or replaces data in a page with existing data. The INTERNAL DATA MOVE command sequence is as follows:

- 13H (PAGE READ TO CACHE)
- 84H/34H(PROGRAM LOAD RANDOM DATA : Optional)
- 06H (WRITE ENABLE)
- 10H (PROGRAM EXECUTE)
- 0FH (GET FEATURE command to read the status)

Prior to performing an INTERNAL DATA MOVE operation, the target page content must be read out into the cache register by issuing a PAGE READ (13H) command. The PROGRAM LOAD RANDOM DATA (84H/34H) command can be issued, if user wants to update bytes of data in the page. This command consists of an 8-bit Op code, followed by 4 dummy bits and a 12-bit column address. New data is loaded in the 12-bit column address. If the RANDOM DATA is not sequential, another PROGRAM LOAD RANDOM DATA (84H/34H) command must be issued with the new column address. After the data is loaded, the WRITE ENABLE command must be issued, then a PROGRAM EXECUTE (10H) command can be issued to start the programming operation.

9.6. ERASE Operation

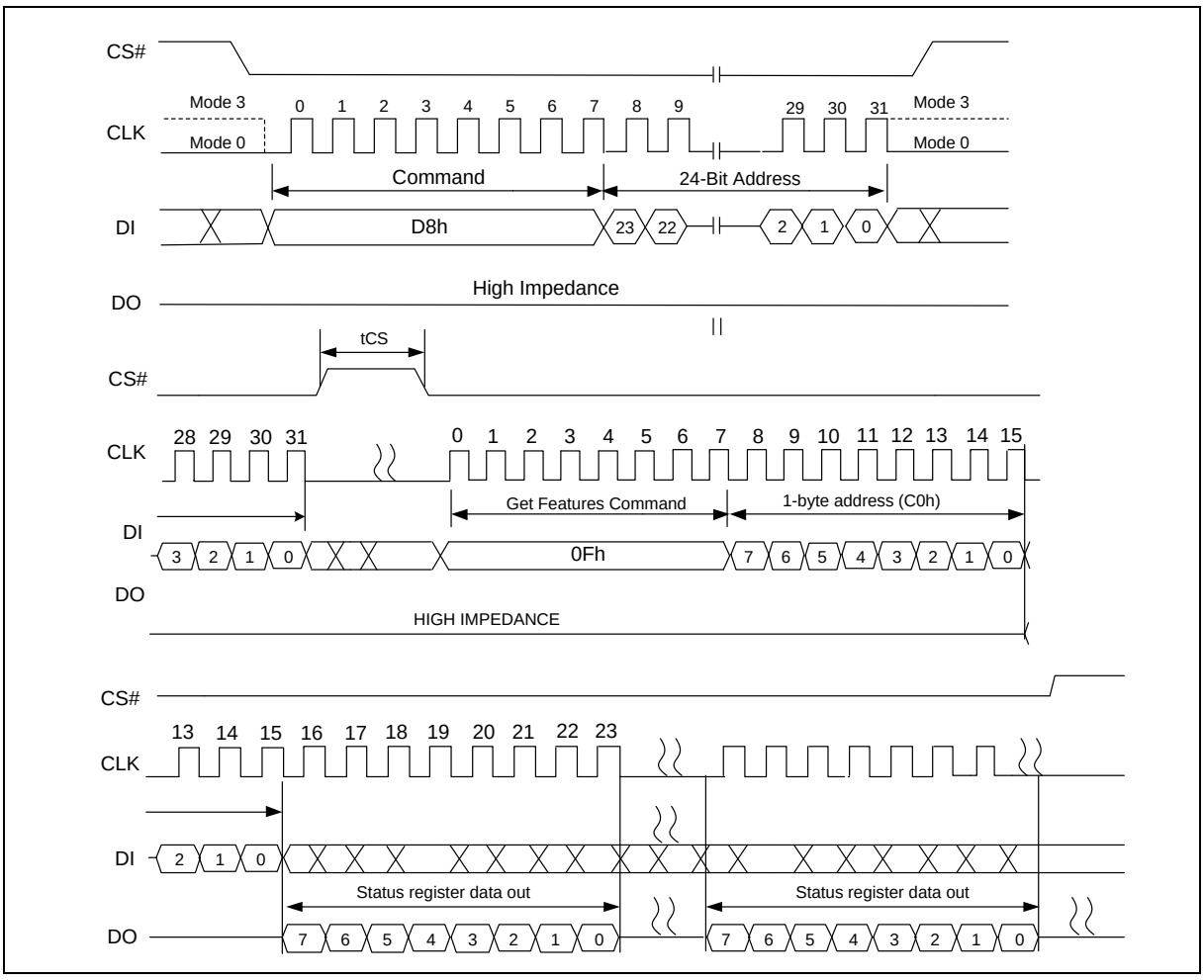
9.6.1. BLOCK ERASE (D8h)

The BLOCK ERASE (D8h) command is used to erase at the block level. The blocks are organized as 64 pages per block, 2176 bytes per page (2048 + 128 bytes). Each block is 136 Kbytes. The BLOCK ERASE command (D8h) operates on one block at a time. The command sequence for the BLOCK ERASE operation is as follows:

- 06h (WRITE ENBALE command)
- D8h (BLOCK ERASE command)
- 0Fh (GET FEATURE command to read the status register)

Prior to performing the BLOCK ERASE operation, a WRITE ENABLE (06h) command must be issued. As with any command that changes the memory contents, the WRITE ENABLE command must be executed in order to set the WEL bit. If the WRITE ENABLE command is not issued, then the rest of the erase sequence is ignored. A WRITE ENABLE command must be followed by a BLOCK ERASE (D8h) command. This command requires a 24-bit address consisting of 7 dummy bits followed by a17-bit row address. After the row address is registered, the control logic automatically controls timing and erase-verify operations. The device is busy for tERS time during the BLOCK ERASE operation. The GET FEATURE (0Fh) command can be used to monitor the status of the operation (refer to the Status Register section).

Figure 25 BLOCK ERASE (D8h) Timing

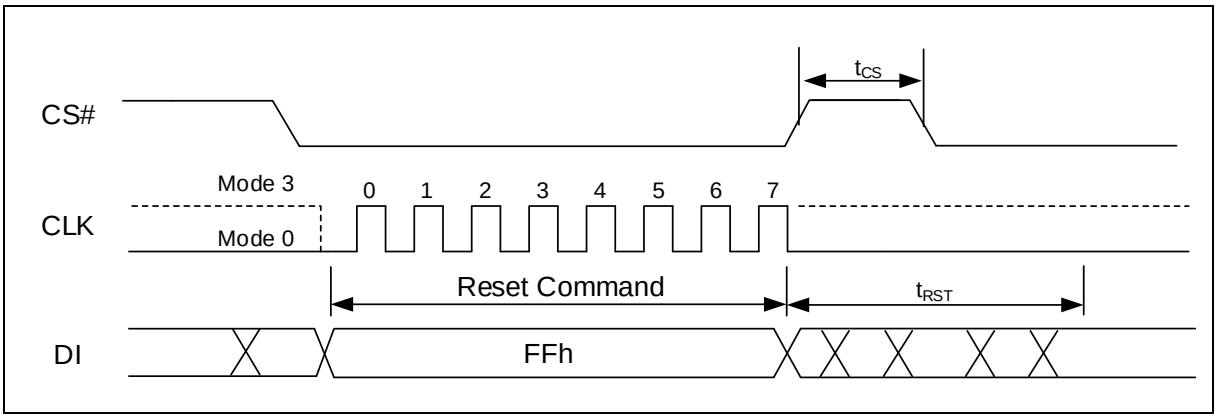


9.7. RESET Operation

9.7.1. RESET (FFh)

The RESET (FFh) command after POWER ON sequence stops all operations. For example, in case of a program or erase or read operation, the reset command can make the device enter the standby state after t_{RST}.

Figure 26 RESET (FFh) Timing



9.8. Write Protection

The write protection will be determined by the combination of TB, BP[3:0] bits in the Block Lock Register (A0h).

Table 9 Block Lock Register Block Protect Bits

CMP	TB	BP2	BP1	BP0	Protected Row Address	Protected Rows
x	X	0	0	0	None	None
0	0	0	0	1	1F800h~1FFFFh	Upper 1/64
0	0	0	1	0	1F000h~1FFFFh	Upper 1/32
0	0	0	1	1	1E000h~1FFFFh	Upper 1/16
0	0	1	0	0	1C000h~1FFFFh	Upper 1/8
0	0	1	0	1	18000h~1FFFFh	Upper 1/4
0	0	1	1	0	10000h~1FFFFh	Upper 1/2
x	X	1	1	1	All (default)	All (default)
0	1	0	0	1	00000h~007FFh	Lower 1/64
0	1	0	1	0	00000h~00FFFh	Lower 1/32
0	1	0	1	1	00000h~01FFFh	Lower 1/16
0	1	1	0	0	00000h~03FFFh	Lower 1/8
0	1	1	0	1	00000h~07FFFh	Lower 1/4
0	1	1	1	0	00000h~0FFFFh	Lower 1/2
1	0	0	0	1	00000h~1F7FFh	Lower 63/64
1	0	0	1	0	00000h~1EFFFh	Lower 31/32
1	0	0	1	1	00000h~1DFFFh	Lower 15/16
1	0	1	0	0	00000h~1BFFFh	Lower 7/8
1	0	1	0	1	00000h~17FFFh	Lower 3/4
1	0	1	1	0	00000h~0003Fh	Block0
1	1	0	0	1	00800h~1FFFFh	Upper 63/64
1	1	0	1	0	01000h~1FFFFh	Upper 31/32
1	1	0	1	1	02000h~1FFFFh	Upper 15/16
1	1	1	0	0	04000h~1FFFFh	Upper 7/8
1	1	1	0	1	08000h~1FFFFh	Upper 3/4
1	1	1	1	0	00000h~0003Fh	Block0

NOTE:
1. X = don’t care
2. Any Erase or Program command for the protected area will be ignored.

10. Unique ID/Parameter/OTP Pages

In addition to the main memory array, the FM25S02BI3 is also equipped with one Unique ID Page, one Parameter Page, and twenty-five OTP Pages.

Page Address	Page Name	Descriptions	Data Length
00h	Unique ID Page	Factory programmed, Read Only	32-ByteX16
01h	Parameter Page	Factory programmed, Read Only	256-ByteX3
02h	OTP Page[0]	Program Only, OTP lockable	2176-Byte
…	OTP Page[1:23]	Program Only, OTP lockable	2176-Byte
1Ah	OTP Page[24]	Program Only, OTP lockable	2176-Byte

To access these additional data pages, the OTP_EN bit in the Status Register-2 must be set to "1" first. Then, Read operations can be performed on the Unique ID and Parameter Pages, Read and Program operations can be performed on the OTP pages if it's not already locked. To return to the main memory array operation, OTP_EN bit needs to be set to 0.

The device offers a protected, One-Time Programmable NAND Flash memory area. Twenty-five full pages (2176 bytes per page) are available on the device, and the entire range is guaranteed to be good. Customers can use the OTP area any way they want, like programming serial numbers, or other data, for permanent storage. When delivered from factory, feature bit OTP_PRT is 0.

To access the OTP feature, the user must issue the SET FEATURE command, followed by feature address B0h. When the OTP is ready for access, pages 02h–1Ah can be programmed in sequential order. The PROGRAM LOAD (02H/32H) and PROGRAM EXECUTE (10H) commands can be used to program the pages. Also, the PAGE READ (13H) command and READ FROM CACHE (03h/0Bh/3Bh/6Bh) commands can be used to read the OTP area. The data bits used in feature address B0h to enable OTP access are shown in the table below.

OTP Access

To access OTP, perform the following command sequence:

- Issue the SET FEATURE command (1Fh) to set OTP_EN
- Issue the PAGE PROGRAM (if OTP_EN=1) or PAGE READ command.

It is important to note that after bits 6 and 7 of the Configuration register are set by the user, the OTP area becomes read-only and no further programming is supported. For OTP states, see the following table.

OTP Protect

- Issue the SET FEATURE command (1FH) to set OTP_EN and OTP_PRT
- 02H command followed by 3-byte 00H (PROGRAM LOAD)
- 06H (WRITE ENABLE)
- Issue the PROGRAM EXECUTE (10H) command
- After power-on, OTP_PRT is 1(OTP_PRT is non-volatile bit). And OTP area is protected.

Table 10 **OTP States**

OTP_PRT	OTP_EN	State
X	0	Normal Operation
0	1	Access OTP region
1	1	Lock the OTP area

10.1. Parameter Page Data Definitions

The Parameter Page contains 3 identical copies of the 256-Byte Parameter Data. The table below lists all the key data byte locations. All other unspecified byte locations have 00h data as default.

Table 11 Parameter Page Definition

Byte Number	Descriptions	Values
0~3	Parameter Page signature	4Fh, 4Eh, 46h, 49h
4~5	Revision number	00h
6~7	Feature supported	00h
8~9	Optional command supported	06h,00h
10~31	Reserved	All 00h
32~43	Device manufacture	46h,55h,44h,41h,4eh,4dh,49h,43h,52h,4fh, 20h, 20h
44~63	Device model	46h,4dh,32h,35h,53h,30h,32h, 42h, 49h,33h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h,20h
64	Manufacture ID	A1h
65~66	Date code	00h,00h
67~79	Reserved	All 00h
80~83	Number of data bytes per page	00h, 08h, 00h, 00h
84~85	Number of spare bytes per page	80h, 00h
86~91	Reserved	All 00h
92~95	Number of pages per block	40h, 00h, 00h, 00h
96~99	Number of blocks per logical unit	00h, 08h, 00h, 00h
100	Number of logical units	01h
101	Number of address bytes	00h
102	Number of bits per cell	01h
103~104	Bad blocks maximum per unit	28h, 00h
105~106	Block endurance	06h,04h
107	Guaranteed valid blocks at beginning of target	01h
108~109	Block endurance for guaranteed valid blocks	01h,03h
110	Number of programs per page	04h
111	Reserved	All 00h
112	Number of ECC bits	00h
113	Number of plane address bits	00h
114	Multi-plane operation attribute	00h
115~127	Reserved	All 00h
128	I/O pin capacitance, maximum	08h
129~132	Reserved	All 00h
133~134	Maximum page program time (μs)	84h,03h
135~136	Maximum block erase time (μs)	10h,27h
137~138	Maximum page read time (μs)	46h,00h
139~163	Reserved	All 00h
164~165	Vendor specified revision number	00h,00h
166~253	Vendor specific	All 00h
254~255	Integrity CRC	Set at test
256~511	Value of bytes 0~255	
512~767	Value of bytes 0~255	
768+	Reserved	

11. Error Management

This NAND Flash device is specified to have the minimum number of valid blocks (NVB) of the total available blocks per die shown in the table below. This means the devices may have blocks that are invalid when shipped from the factory. An invalid block is one that contains at least one page that has more bad bits than can be corrected by the minimum required ECC. Additional bad blocks may develop with use. However, the total number of available blocks will not fall below NVB during the endurance life of the product.

Although NAND Flash memory devices may contain bad blocks, they can be used reliably in systems that provide bad-block management and error-correction algorithms. This ensures data integrity.

Internal circuitry isolates each block from other blocks, so the presence of a bad block does not affect the operation of the rest of the NAND Flash array.

NAND Flash devices are shipped from the factory erased. The factory identifies invalid blocks before shipping by attempting to program the bad-block mark into every location in the first and second page of each invalid block. It may not be possible to program every location in an invalid block with the bad-block mark. However, the first spare area location (800h) in each bad block is guaranteed to contain the bad-block mark. This method is compliant with ONFI factory defect mapping requirements. See the following table for the bad-block mark.

System software should initially check the first spare area location (800h) for non-FFh data on the page 0 and page 1 of each block prior to performing any program or erase operations on the NAND Flash device. A bad-block table can then be created, enabling system software to map around these areas. Factory testing is performed under worst-case conditions. Because invalid blocks may be marginal, it may not be possible to recover the bad-block marking if the block is erased.

Table 12 Error Management Details

Description	Requirement
Minimum number of valid blocks (N_{VB})	2008
Total available blocks per die	2048
First spare area location	Column 2048 of page 0 and page 1
Bad-block mark	Non FFh

12. ECC Protection

The device offers data corruption protection by offering optional internal ECC. READs and PROGRAMs with internal ECC can be enabled or disabled by setting feature bit ECC_E. ECC is enabled after device power up, so the default READ and PROGRAM commands operate with internal ECC in the active state.
To enable/disable ECC, perform the following command sequence:

- Issue the SET FEATURE command (1FH).
- Set the feature bit ECC_E as you want:
  1. To enable ECC, Set ECC_E to 1.
  2. To disable ECC, Clear ECC_E to 0.

During a PROGRAM operation, the device calculates an ECC code on the 2k page in the cache register, before the page is written to the NAND Flash array.
During a READ operation, the page data is read from the array to the cache register, where the ECC code is calculated and compared with the ECC code value read from the array. If error bits are detected, the error is corrected in the cache register. Only corrected data is output on the I/O bus. The ECC status bit indicates whether or not the error correction was successful. The ECC Protection table below shows the ECC protection scheme used throughout a page.

The device will automatically read first page of first block to cache after power on, then host can directly read data from cache for easy boot. Also the data is promise correctly by internal ECC.

With internal ECC, the user must accommodate the following:

- Spare area definitions provided in the ECC Protection table below.
- ECC can protect according main and spare areas.

Table 13 ECC Protection and Spare Area

Min Byte Address	Max Byte Address	ECC Protected	Number Of Bytes	Area	Description
000H	1FFH	Yes	512	Main 0	User data 0
200H	3FFH	Yes	512	Main 1	User data 1
400H	5FFH	Yes	512	Main 2	User data 2
600H	7FFH	Yes	512	Main 3	User data 3
800H	801H	NO	2		Reserved (bad block mark)
802H	803H	NO	2	Spare 0	User meta data II
804H	80FH	Yes	12	Spare 0	User meta data I
810H	811H	NO	2		Reserved
812H	813H	NO	2	Spare 1	User meta data II
814H	81FH	Yes	12	Spare 1	User meta data I
820H	821H	NO	2		Reserved
822H	823H	NO	2	Spare 2	User meta data II
824H	82FH	Yes	12	Spare 2	User meta data I
830H	831H	NO	2		Reserved
832H	833H	NO	2	Spare 3	User meta data II
834H	83FH	Yes	12	Spare 3	User meta data I
840H	87FH	Yes	64	Spare Area(1)	Internal ECC parity data

NOTE:
1. When ECC_E=1, Spare area is only for internal ECC.
   When ECC_E=0, Spare area can be used as user data.
2. Spare 800h byte for bad block marker

13. Electrical Characteristics

13.1. Absolute Maximum Ratings

Table 14 Absolute Maximum Ratings

Operating Temperature	-40°C to +85°C
Storage Temperature	-65°C to +150°C
Voltage on I/O Pin with Respect to Ground	-0.5V to 4.0V
V_{CC}	-0.5V to 4.0V

Note: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

13.2. Pin Capacitance

Table 15 Pin Capacitance

Applicable over recommended operating range from: T_A = 25°C

Symbol	Test Condition	Max	Units	Conditions
C_{IN} (1)	Input Capacitance	8	pF	V_{IN} = 0V
C_{OUT} (1)	Output Capacitance	8	pF	V_{OUT} = 0V

Note: 1. Characterized and is not 100% tested.

13.3. Power-up Timing

Figure 27 Power-On Timing

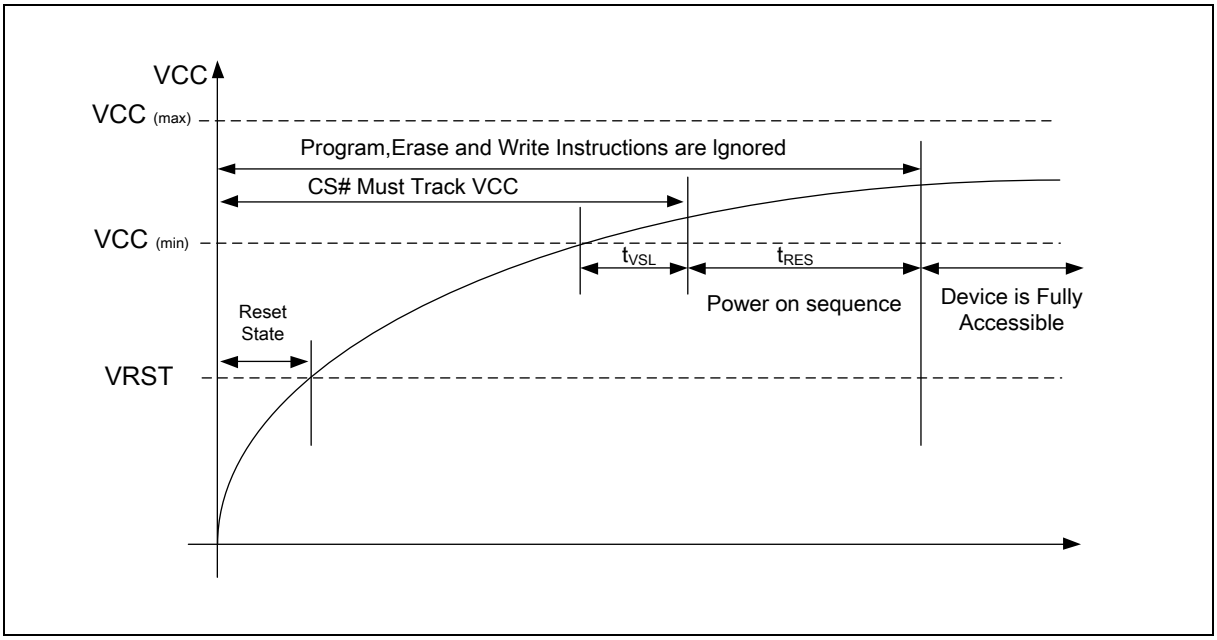


Table 16 Power-On Timing and Write Inhibit Threshold

PARAMETER	SYMBOL	SPEC		UNIT
		MIN	MAX	
VCC (min) to CS# Low	t_{VSL}	1		ms
Power on sequence	t_{RES}	1		ms
Chip Reset Voltage	V_{RST}		2.5	V

13.4. DC Electrical Characteristics

Table 17 DC Characteristics

Applicable over recommended operating range from: T_A = -40°C to 85°C, V_{CC} = 2.7V to 3.6V.

SYMBOL	PARAMETER	CONDITIONS	SPEC			UNIT
			MIN	TYP	MAX	
V_{CC}	Power supply for 3.3V mode		2.7		3.6	V
I_{LI}	Input Leakage Current				±10	µA
I_{LO}	Output Leakage Current				±10	µA
I_{SB1}	Standby Current	VCC= V_{Ccmax}, CS# =VCC, V_{IN} = VSS or VCC		10	50	µA
I_{CC1}	Operating Current	CLK=0.1VCC/0.9VCC F_{CLK}=F_{Cmax}, Read			20	mA
I_{CC2}		Program			20	mA
I_{CC3}		Erase			20	mA
V_{IL}(1)	Input Low Voltage		-0.3		0.2V_{CC}	V
V_{IH}(1)	Input High Voltage		0.7V_{CC}		V_{CC}+0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 1.6mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = -100 µA	V_{CC}-0.2			V

Notes:

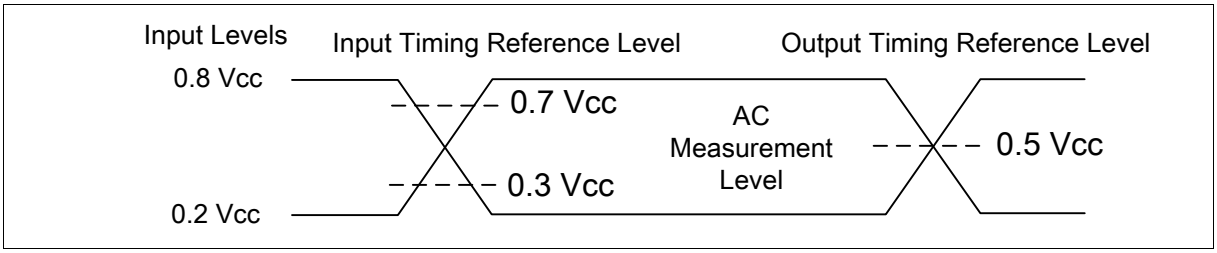
1. V_{IL}min and V_{IH}max are reference only and are not tested.

13.5. AC Measurement Conditions

Table 18 AC Measurement Conditions

SYMBOL	PARAMETER	SPEC		UNIT
		MIN	MAX	
CL	Load Capacitance		15	pF
TR, TF	Input Rise and Fall Times		5	ns
VIN	Input Pulse Voltages	0.2 V_{CC} to 0.8 V_{CC}		V
IN	Input Timing Reference Voltages	0.3 V_{CC} to 0.7 V_{CC}		V
OUT	Output Timing Reference Voltages	0.5V_{CC}		V

Figure 28 AC Measurement I/O Waveform



13.6. AC Electrical Characteristics

Table 19 AC Characteristics

Applicable over recommended operating range from: T_A = -40°C to 85°C, V_{CC} = 2.7V to 3.6V, (unless otherwise noted).

SYMBOL	PARAMETER	SPEC			UNIT
		MIN	TYP	MAX	
F_C	Serial Clock Frequency for all other instructions			104	MHz
t_{CH1}(1)	Serial Clock High Time	4.5			ns
t_{CL1}(1)	Serial Clock Low Time	4.5			ns
t_{CLCH}(2)	Serial Clock Rise Time (Slew Rate)	0.1			V/ns
t_{CHCL}(2)	Serial Clock Fall Time (Slew Rate)	0.1			V/ns
t_{SLCH}	CS# Active Setup Time	5			ns
t_{CHSH}	CS# Active Hold Time	5			ns
t_{SHCH}	CS# Not Active Setup Time	5			ns
t_{CHSL}	CS# Not Active Hold Time	5			ns
t_{SHSL}/t_{CS}	CS# High Time	80			ns
t_{SHQZ}(2)	Output Disable Time			20	ns
t_{CLQX}	Output Hold Time	1.5			ns
t_{DVCH}	Data In Setup Time	2			ns
t_{CHDX}	Data In Hold Time	3			ns
t_{HLCH}	HOLD# Low Setup Time (relative to CLK)	4.5			ns
t_{HHCH}	HOLD# High Setup Time (relative to CLK)	4.5			ns
t_{CHHH}	HOLD# High Hold Time (relative to CLK)	4.5			ns
t_{CHHL}	HOLD# Low Hold Time (relative to CLK)	4.5			ns
t_{HLQZ}(2)	HOLD# Low to High-Z Output			8	ns
t_{HHQX}(2)	HOLD# High to Low-Z Output			8	ns
t_{CLQV}	Output Valid from CLK			8	ns
t_{WHSL}	WP# Setup Time before CS# Low	20			ns
t_{SHWL}	WP# Hold Time after CS# High	100			ns
t_{RST}	Resetting time during Idle/Read/Program/Erase			5/5/10 /500	µs

Notes:

1. $T_{CH1}+T_{CL1} >= 1 / F_C$;
2. characterized and not 100% tested.

Table 20 Performance Timing

SYMBOL	PARAMETER	SPEC			UNIT
		MIN	TYP	MAX	
t_{RD}	Page Read From Array (with ECC)			70	µs
	Page Read From Array (without ECC)			25	
t_{PROG}	Page Program		400	900	µs
t_{ERS}	Block Erase		4	10	ms

Figure 29 Serial Output Timing

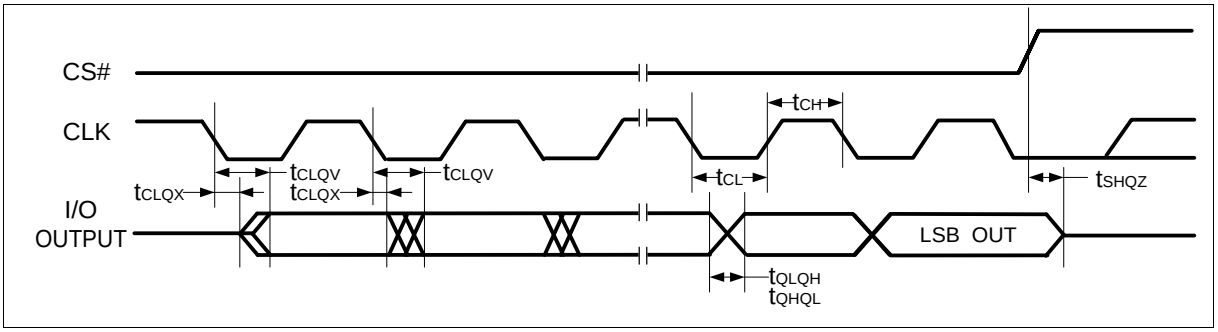


Figure 30 Serial Input Timing

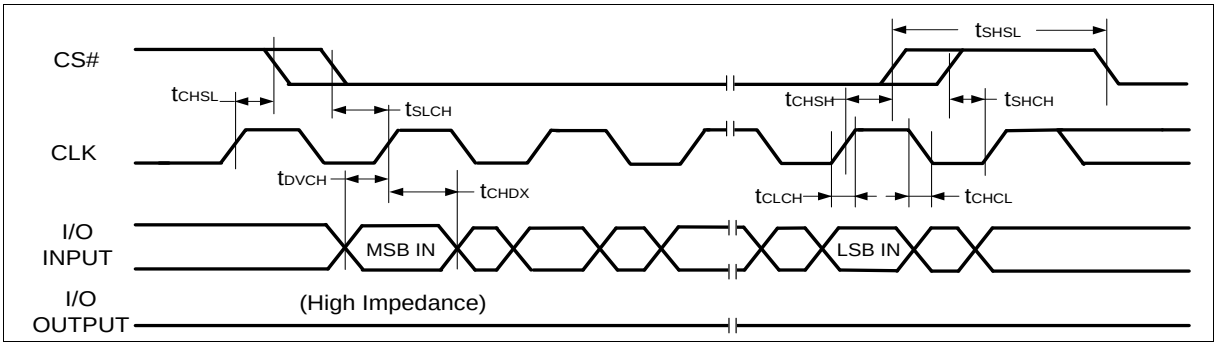


Figure 31 Hold Timing

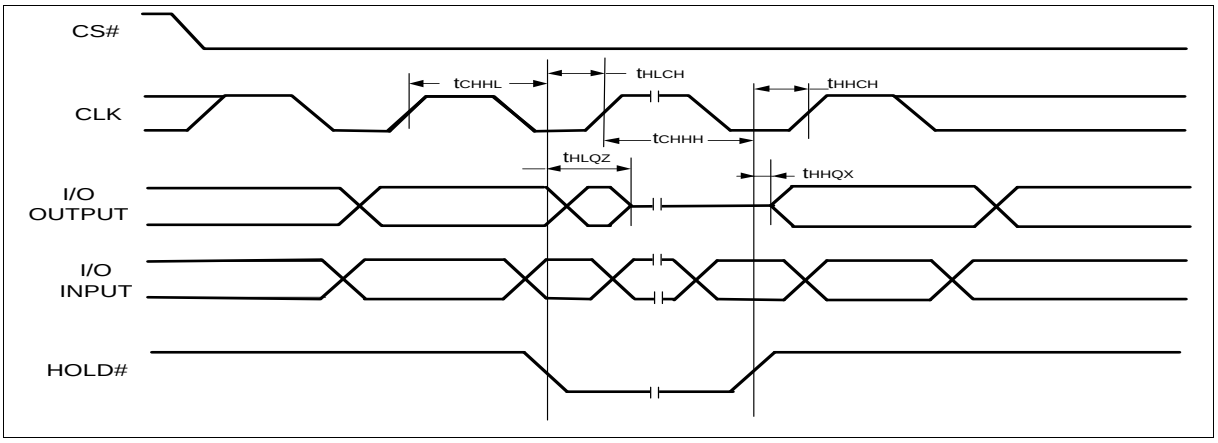
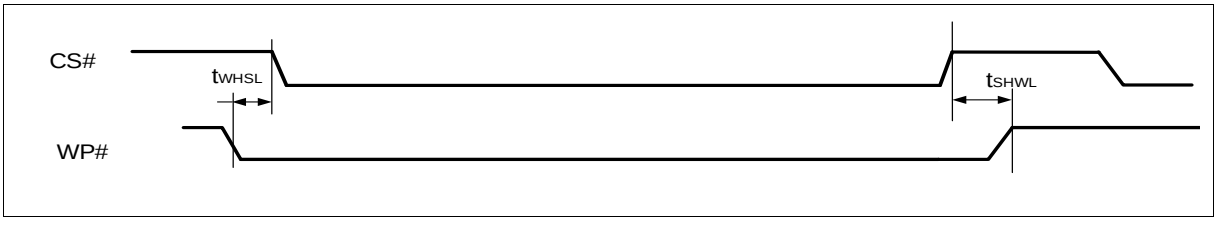
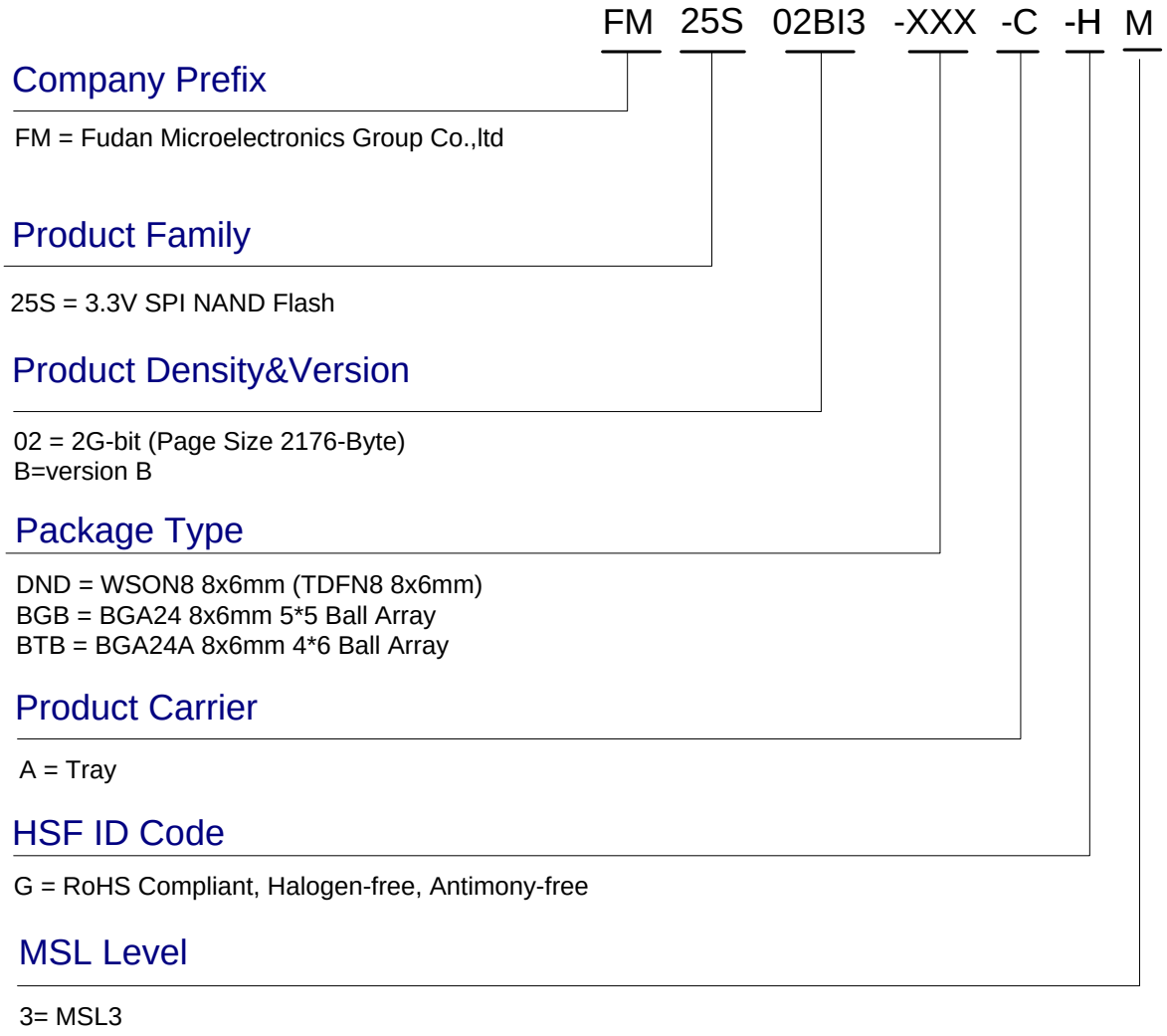


Figure 32 WP Timing

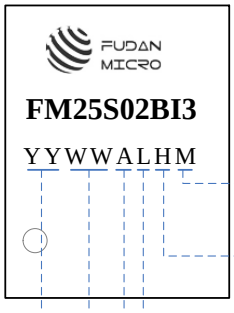


14. Ordering Information



15. Part Marking Scheme

WSON8 8x6mm (TDFN8 8x6mm)



Moisture Sensitivity Level
Blank=MSL3

HSF ID Code
G = RoHS Compliant, Halogen-free, Antimony-free

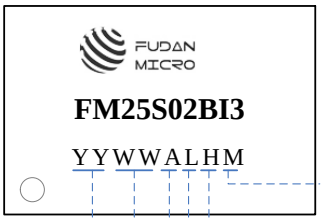
Lot Number（just with 0~9、A~Z）

Assembly's Code

Work week during which the product was molded (eg..week 12)

The last two digits of the year In which the product was sealed / molded.

BGA24 8x6mm 5*5 Ball Array



Moisture Sensitivity Level
Blank=MSL3

HSF ID Code
G = RoHS Compliant, Halogen-free, Antimony-free

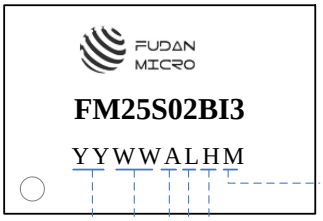
Lot Number（just with 0~9、A~Z）

Assembly's Code

Work week during which the product was molded (eg..week 12)

The last two digits of the year In which the product was sealed / molded.

BGA24A 8x6mm 4*6 Ball Array



Moisture Sensitivity Level
Blank=MSL3

HSF ID Code
G = RoHS Compliant, Halogen-free, Antimony-free

Lot Number（just with 0~9、A~Z）

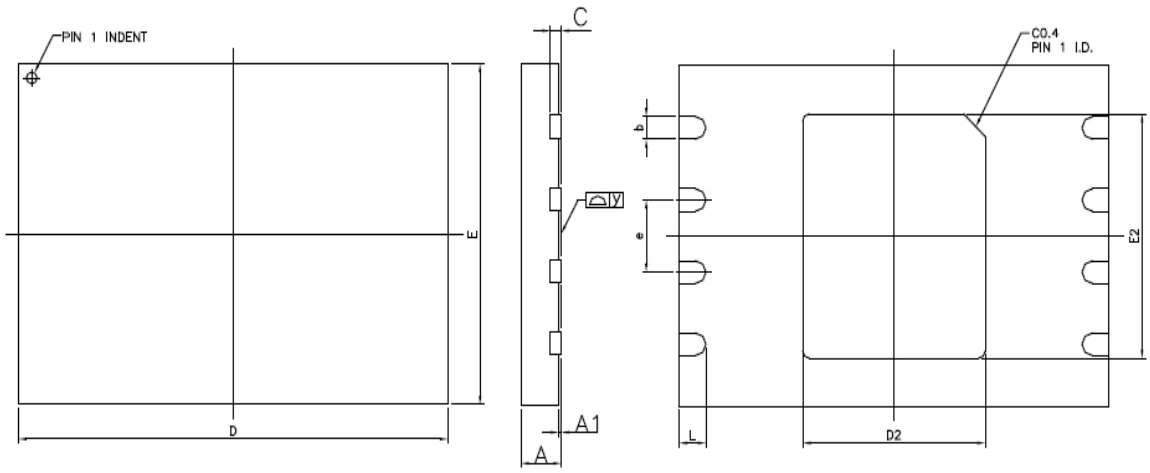
Assembly's Code

Work week during which the product was molded (eg..week 12)

The last two digits of the year In which the product was sealed / molded.

16. Packaging Information

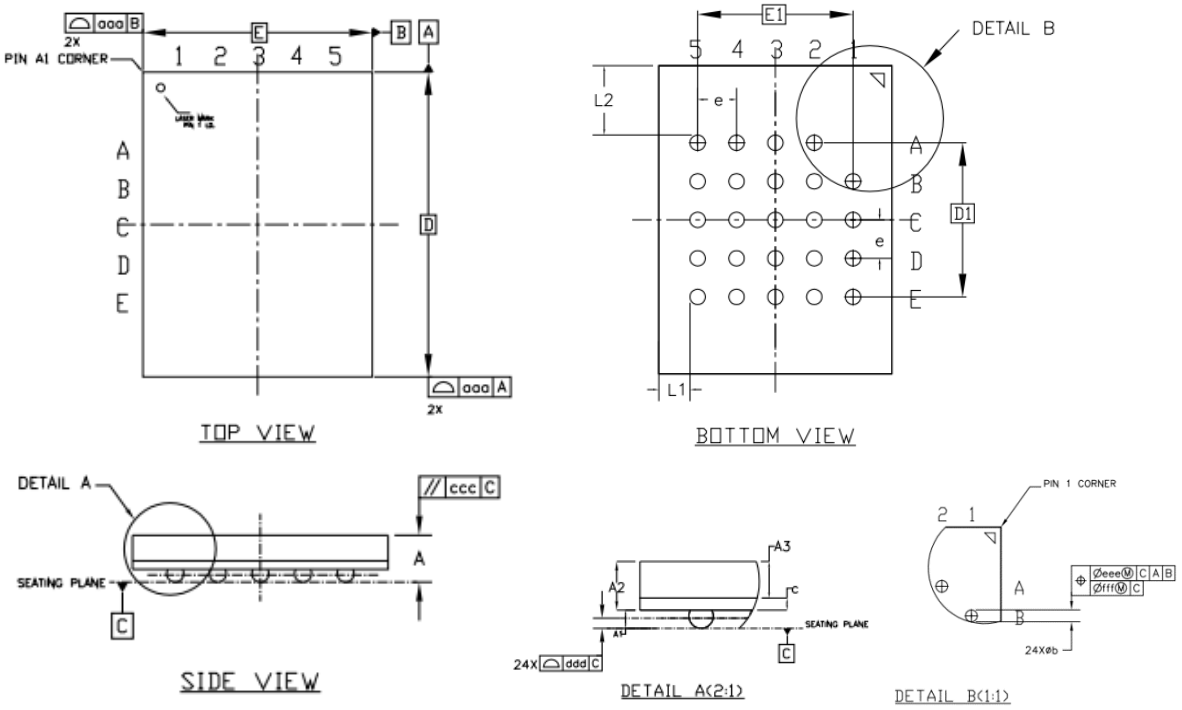
WSON8 8x6mm (TDFN8 8x6mm)



Symbol	MIN	NOM	MAX
e		1.270 BSC	
D	7.900	8.000	8.100
E	5.900	6.000	6.100
L	0.400	0.500	0.600
A	0.700	0.750	0.800
A1	0.000	0.025	0.050
C		0.200 REF	
b	0.350	0.400	0.450
D2	3.300	3.400	3.500
E2	4.200	4.300	4.400

Note:
1. Dimensions are in Millimeters.

BGA24 8x6mm 5*5 Ball Array

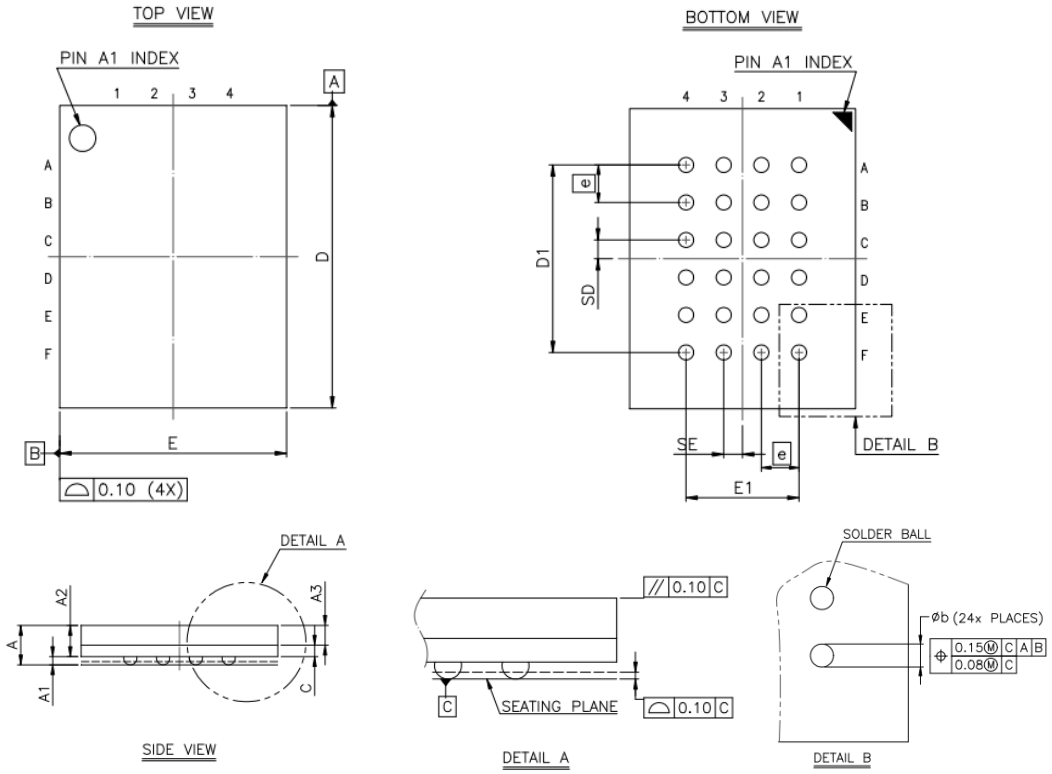


Symbol	MIN	NOM	MAX
A	---	---	1.200
A1	0.250	0.300	0.350
A2		0.790 BSC	
D	7.900	8.000	8.100
D1		4.000 BSC	
E	5.900	6.000	6.100
E1		4.000 BSC	
e		1.000 BSC	
b	0.350	0.400	0.450

Note:

1. Dimensions are in Millimeters.

BGA24A 8x6mm 4*6 Ball Array



Symbol	MIN	NOM	MAX
A	---	---	1.200
A1	0.250	0.300	0.350
A2		0.790 BSC	
D	7.900	8.000	8.100
D1		5.000 BSC	
E	5.900	6.000	6.100
E1		3.000 BSC	
e		1.000 BSC	
b	0.350	0.400	0.450

Note:

1. **Dimensions are in Millimeters.**

17. Revision History

Version	Publication date	Pages	Paragraph or Illustration	Revise Description
preliminary	Jul.2023	47		Initial Document Release
1.0	Mar.2024	45		Add BGA24 package
1.1	April.2024	43		Modify t_{HLQZ} and t_{HLQZ}

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